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Microcontroller Based Implementation of Multi-Level Inverter Based Dynamic Voltage Restorer

N.S.Sakthivel Murugan[1] A.Nirmal Kumar[2] T.Vijayakumar[3]

Abstract – This paper deals with simulation and implementation of multilevel inverter based Dynamic Voltage Restorer (DVR). The DVR circuit produces high quality voltage since it uses a nine level inverter. This DVR gives better solution to the voltage sag problem by injecting a voltage with reduced harmonics. DVR controls the voltage applied to the load by injecting voltage of proper amplitude and phase angle. Thus DVR is responsible for restoring quality of voltage derived to the end user.

Keywords – DVR, Multi-level inverter, MATLAB.

I. INTRODUCTION

Power electronic devices contribute an important part of harmonics in all kind of applications, such as power rectifiers, thyristor converters, and static VAr compensators (SVC). The updated pulse-width modulation (PWM) techniques used to control modern static converters such as machine derives, power factor compensators, or active power filters do not produce perfect waveforms, which strongly depend on the semiconductors switching frequency. Voltage or current converters as they generate discrete output waveforms, force the use of machines with special isolation, and in some applications large inductances connected in series with the respective load. In other words, neither the voltage nor the current waveforms are as expected. Also, it is well known that distorted voltages and current waveforms produce harmonic contamination, additional power losses, and high frequency noise that can affect not only the power load but also the associated controllers. All these unwanted operating characteristics associated with PWM converters can be overcome with multilevel converters, in addition to the fact that higher voltage levels can be achieved[1]-[5].

Multilevel inverters can operate not only with PWM techniques but also with amplitude modulation (AM), significantly improving the quality of the output voltage waveform. With the use of AM, low frequency voltage harmonics are perfectly eliminated, generating almost perfect sinusoidal waveforms with a total harmonic distortion (THD) lower than 5%. Another important characteristic is that each converter operates at a low switching frequency, reducing the semiconductor stresses, and therefore reducing the switching losses [6], [7]. The principal objective of this paper is to determine the simplest converter topology in terms of the number of power semiconductors for a given number of levels. The "redundant" levels are minimized, and the combination of bridges to maximize the number of levels [8], [9] and minimize power sources and semiconductors are analyzed.

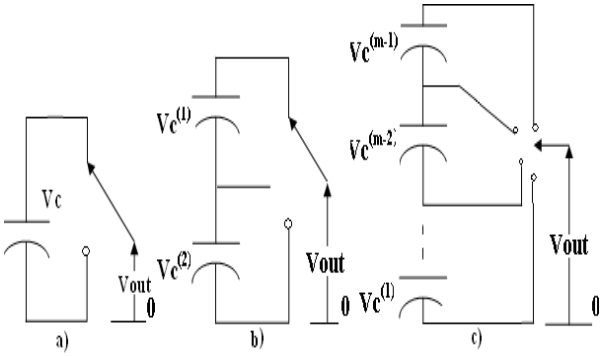

Fig. 1: Basic multi-level inverters (a) two levels, (b) three levels and (c) m levels

II. MULTI-LEVEL CONVERTER CHARACTERISTICS

The principal function of the inverters is to generate an AC voltage from a DC source voltage. If the DC voltage sources connected in series, it becomes possible to generate an output voltage with several steps. Multilevel inverters include an arrangement of semiconductors and DC voltage sources required to generate a staircase output voltage waveform. Fig. 1 shows the schematic diagram of voltage source-inverters with a different number of levels. It is well known that a two level inverter, such as the one shown in Fig. 1(a), generates an output voltage with two different values (levels) Vc and "zero", with respect to the negative terminal of the DC source ("0"), while a three-level module, Fig, 1(b) generates three different voltages at the output (2Vc, Vc and "zero"). The different positions of the ideal switches are implemented with a number of semiconductors that are in direct relation with the output voltage number of levels.

Multilevel inverters are implemented with small DC sources to form a staircase ac waveform, which follows a given reference template. For example, having ten DC sources with magnitudes equal to 20 V each a composed 11-level waveform can be obtained (five positive, five negatives and zero with respect to the middle point between the ten sources), generating a sinusoidal waveform with 100 V amplitude as shown in Fig. 2, and with very low THD.

It can be observed that the larger the number of the inverter DC supplies, the greater the number of steps that can be generated, obtaining smaller harmonic distortion. However the number of DC sources is directly related to the number of levels through the equation:

$$n = m - 1 \quad (1)$$

where n is the number of DC supplies connected in series and m is the number of the output voltage levels. In order to

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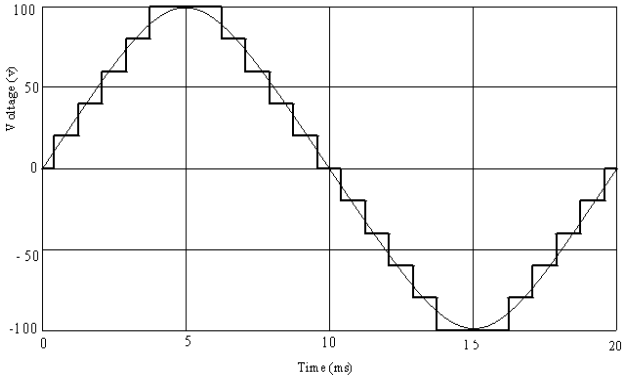


Fig. 2: Voltage waveform from an 11-level inverter

get a 51-level inverter output voltage, 5C-V supplies would be required, which is too much for a simple topology.

Besides the problem of having to use too many power supplies to get a multilevel inverter, there is a second problem which is also important, the number of power semiconductors required to implement the commutator, as shown in Fig 1. Technical literature has proposed two converter topologies for the implementation of the power converter, using force-commutated devices [transistors or gate turnoffs (GTOs)]: a) the diode-clamped and b) the capacitor-clamped converter [2]. The above work does not use multi-level inverter in the DVR system. This work suggests nine-level inverter based DVR for the control of reactive power. The literature [1] to [10] do not deal with embedded implementation of DVR. This paper presents PIC embedded controller based multilevel inverter fed DVR system.

A. Diode-Clamped Inverter

This inverter consists of a number of semiconductors connected in series, and another identical number of voltage sources, also connected in series. These two chains are connected with diodes at the upper and lower semiconductors as shown in Fig 3 (a). For an m-level converter, the requires number of transistors T is given by

$$T = 2 (m – 1) \qquad (2)$$

Then, for example of a 51-level converter, 100 power transistors would be required (which is an enormous amount of switches to be controlled). One of the most utilized configurations with this topology is that of the three-level inverter, which is shown in Fig. 3 (b). The capacitors act like two DC sources connected in series. Thus, in the diagram, each capacitor accumulates ½ V_{DC}, giving voltages at the output of ½ V_{DC}, 0, or - ½ V_{DC} with respect to the middle point between the capacitors.

B. Capacitor-Clamped Inverter

This inverter has a similar structure to that of the diode-clamped, however it can generate the voltage steps with capacitors connected as shown in Fig 4. The problem with this converter is that it requires a large number of capacitors, which translates is that it requires a large number of capacitors, which translates to a bulky and expensive converter as compared with the diode-clamped inverter. Besides, the number of transistors used is the same with the diode-clamped inverter, and therefore, for a 51-level inverter,

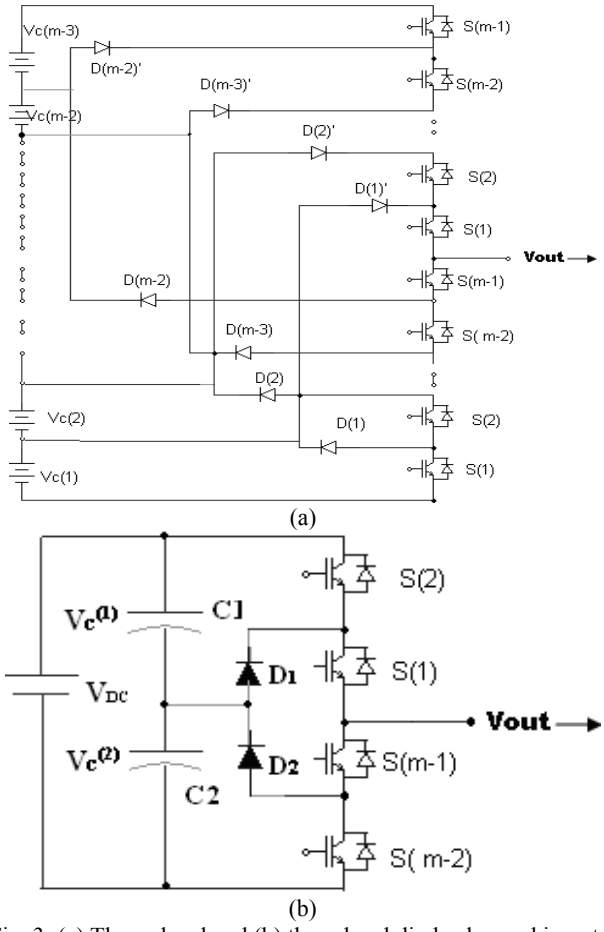


Fig. 3: (a) The m-level and (b) three-level diode clamped inverter topology

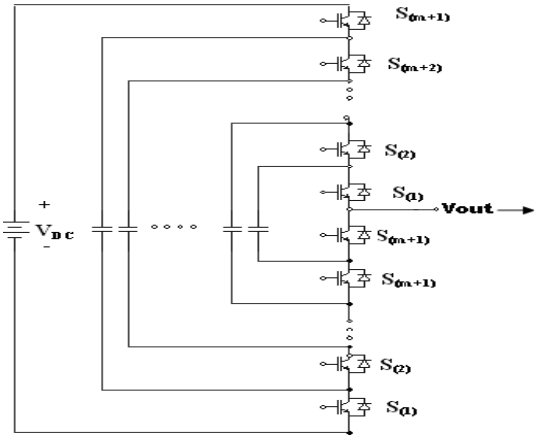


Fig. 4: The m-level capacitor – clamped inverter

100 power transistors are required. In order to overcome all these problems, a third topology, which will be called the "transistor-clamped inverter" will be presented and analyzed.

C. Transistor-Clamped Inverter:

The transistor-clamped inverter has the advantage of requiring the same number of power transistors as the levels generated, and therefore, the semiconductors are reduced by half with respect to the previous topologies. A 51-level converter requires 51 transistors (instead of 100 transistors). For an m-level transistor clamped inverter, which satisfies

$$T = m. \qquad (3)$$

in this topology, the control of the gates is very simple

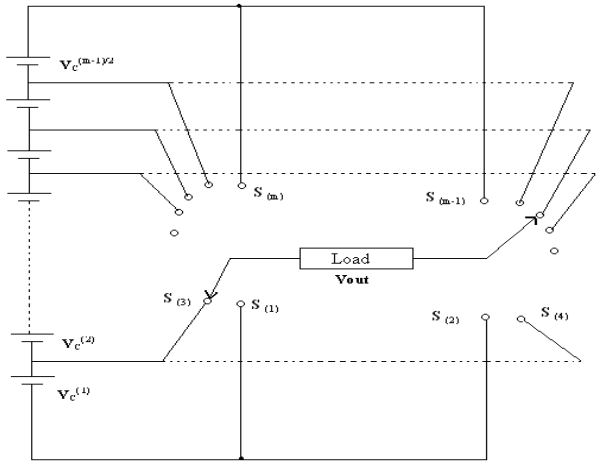


Fig. 5: The m-level inverter using an 'H' bridge

because only one power transistor is switched-on at a time. Then, there is a direct relation between the output voltage, V_{out} and the transistor that has to be turned-on. However, and despite the excellent characteristics of this topology, the number of transistors is still too large to allow the implementation of a practical converter with more than 50 levels.

One solution for increasing the number of steps could be the use of "H" converters, like the one shown in Fig. 5, which consists of connecting two of the previously discussed topologies in series (two legs). If transistor-clamped inverters are used to build an "H" converter, the number of transistors required for an m-level inverter is m+1, which means only one more transistor than what is required for a simple leg configuration. However, the number of DC source is reduced to 50%, which is the most important advantage of "H" converters.

Another characteristic is that the "H" topology has many redundant combinations of switch positions to produce the same voltage levels. As an example, the level "zero" can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on. Another characteristic of "H" converters is that they only produce an odd number of levels, which ensures the existence of the "0-V" level at the load.

For example, a 51-level inverter using an "H" configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

III. Simulation of Cascaded Nine-Level Inverter

The cascaded nine-level inverter has been simulated using MATLAB software. The simulation circuit is illustrated in Fig. 6a. The voltage of the cascaded nine-level inverter can be synthesized from the following switching combinations. The table 1 shows the switching sequence. Driving pulse sequence is selected such that nine-level output is obtained. The driving pulses for switches S1 and S2 are shown in following Fig. 6b. The driving pulses for switches S5 and S6 are shown in Fig. 6c. The Fig. 6d shows the output voltage across inverter 1. The Fig. 6e shows the output voltage across inverter 2. Nine-level inverter output is shown in Fig. 6f. The frequency spectrum for the output of the inverter is shown in Fig. 6g. The value of THD is 19.6%. in three-phase inverter THD is further reduced due to the absence of third harmonic voltage

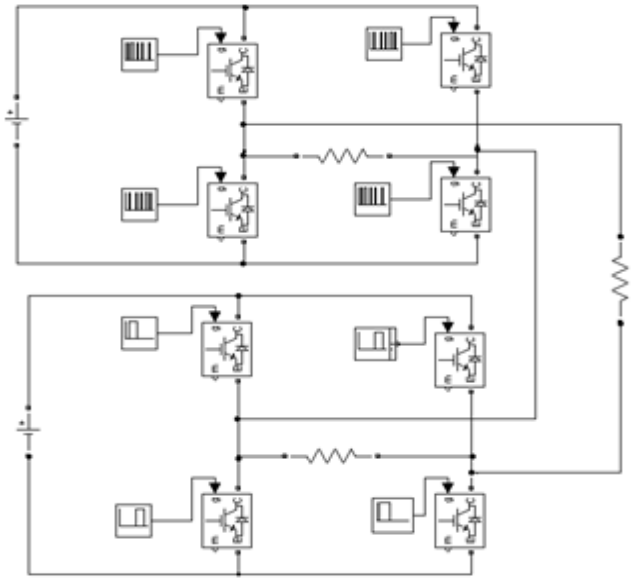


Fig. 6a: Simulation circuit of cascaded nine-level inverter

Table 1: Switching sequence

Output Voltage (V)	SWITCHING SEQUENCE							
	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	0	0	0	0	0	0
V1	1	1	0	0	0	0	0	0
V2	0	0	1	1	1	1	0	0
V3	0	0	0	0	1	1	0	0
V4	1	1	0	0	1	1	0	0
V3	0	0	0	0	1	1	0	0
V2	0	0	1	1	1	1	0	0
V1	1	1	0	0	0	0	0	0
-V1	0	0	1	1	0	0	0	0
-V2	1	1	0	0	0	0	1	1
-V3	0	0	0	0	0	0	1	1
-V4	0	0	1	1	0	0	1	1
-V3	0	0	0	0	0	0	1	1
-V2	1	1	0	0	0	0	1	1
-V1	0	0	1	1	0	0	0	0

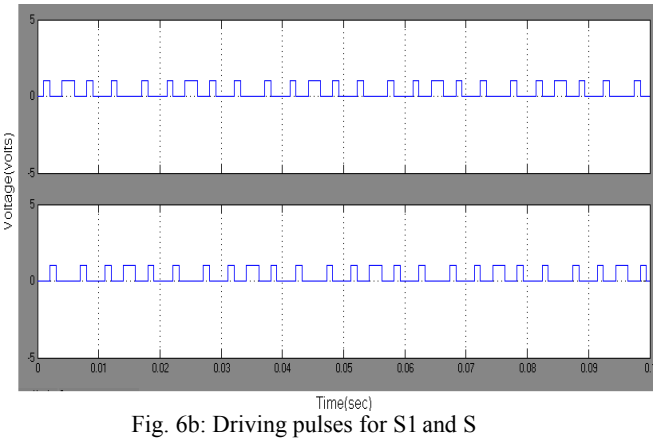


Fig. 6b: Driving pulses for S1 and S

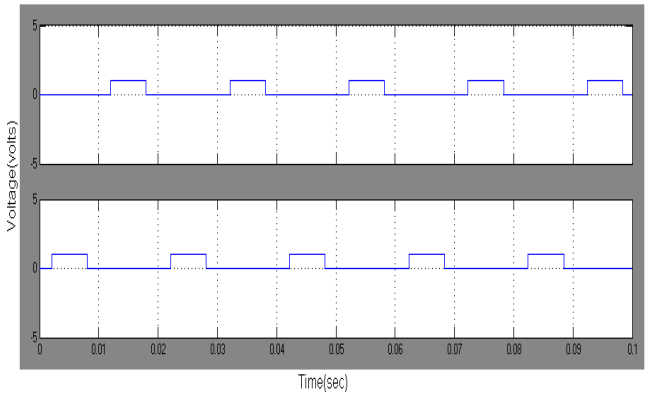


Fig. 6c: Driving pulses for S_5 and S_6

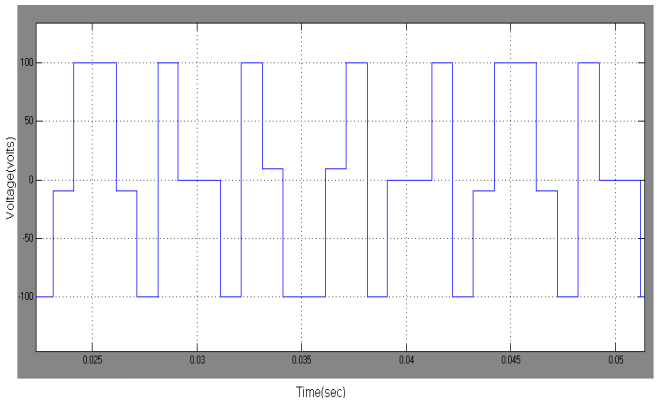


Fig. 6d: Output voltage across inverter-1

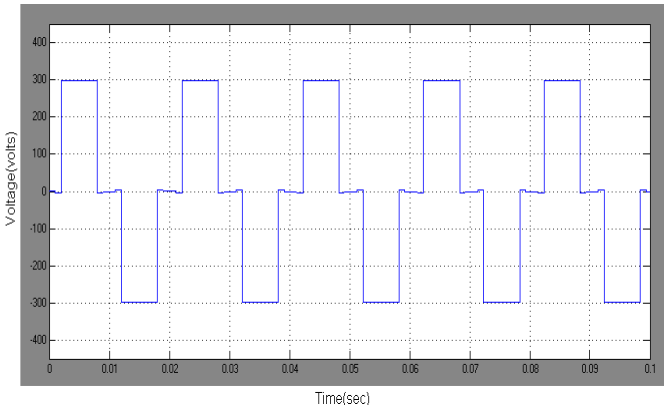


Fig. 6e: Output voltage across inverter-2

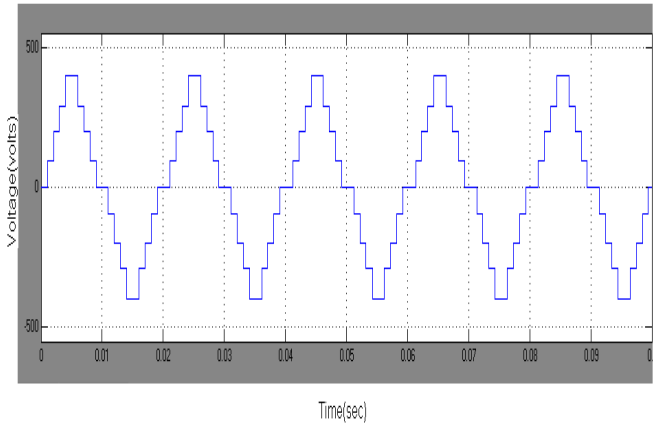


Fig. 6f: Output of nine-level inverter

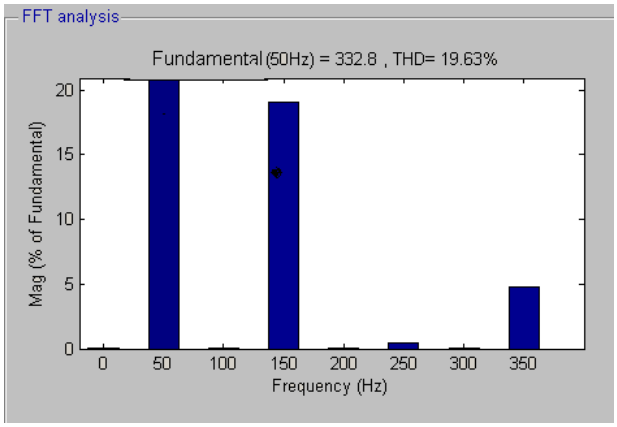


Fig. 6g: Frequency spectrum for output voltage

IV. Experimental Results

A laboratory model for nine- level inverter is fabricated and tested. Experimental set up is shown in Fig. 7a. The hardware consists of power supply board, MOSFET board and driver IC board. The pulses required by the MOSFETs are generated by using microcontroller PIC16F84A. The pulses are amplified using the driver IC IR2110 Driving pulses for S1 and S5 are shown in Figs. 7b and 7c respectively. Output voltages of inverter 1 and 2 are shown in Fig. 7d. Output of inverter 2 is shown in Fig. 7e. Nine-level output is shown in Fig. 7f. The control circuit is shown in Fig. 7g. The flow chart and delay subroutine for the microcontroller are shown in Figs. 7h and 7i

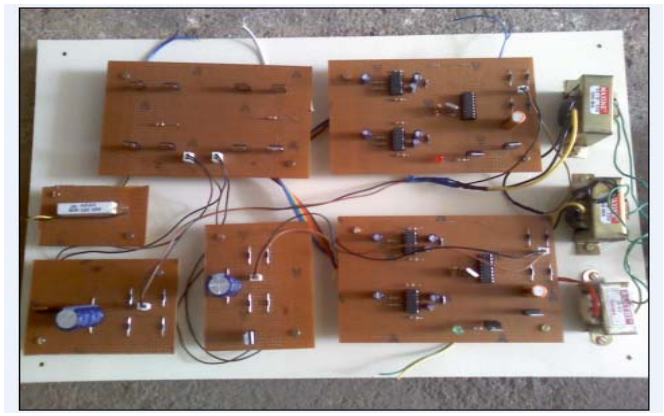


Fig. 7a: Experimental Setup

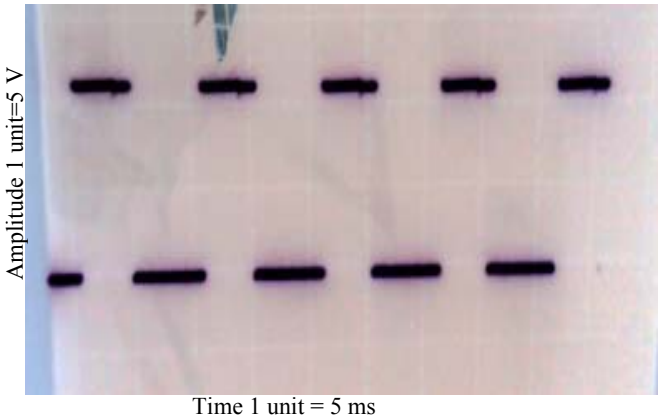
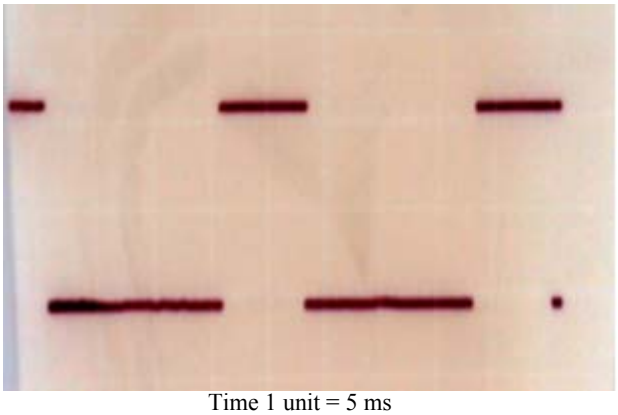
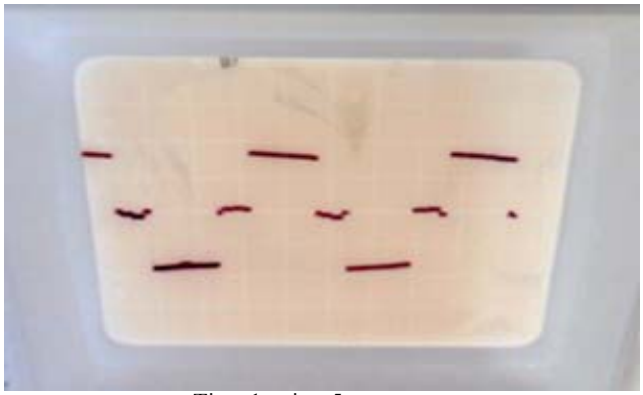


Fig. 7b: Driving pulse for S1



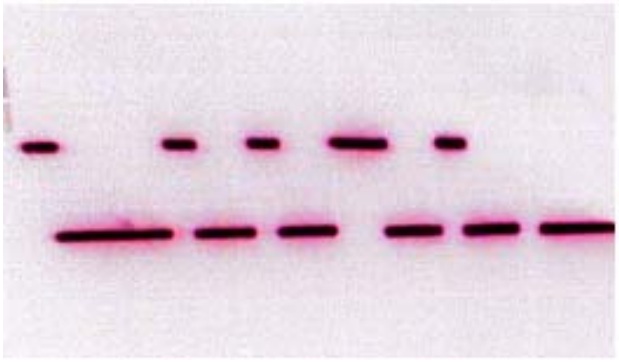
Time 1 unit = 5 ms

Fig. 7c: Driving pulse for S5



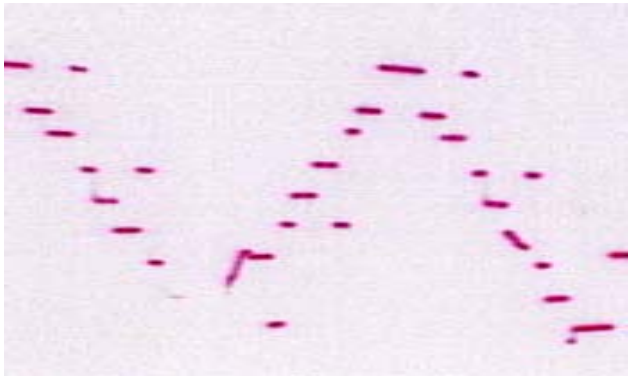
Time 1 unit = 5 ms

Fig.7e: Output voltage of Inverter-2



Time 1 unit = 5 ms

Fig. 7d: Output voltage of Inverter-1



Time 1 unit = 5 ms

Fig. 7f: Nine-level output

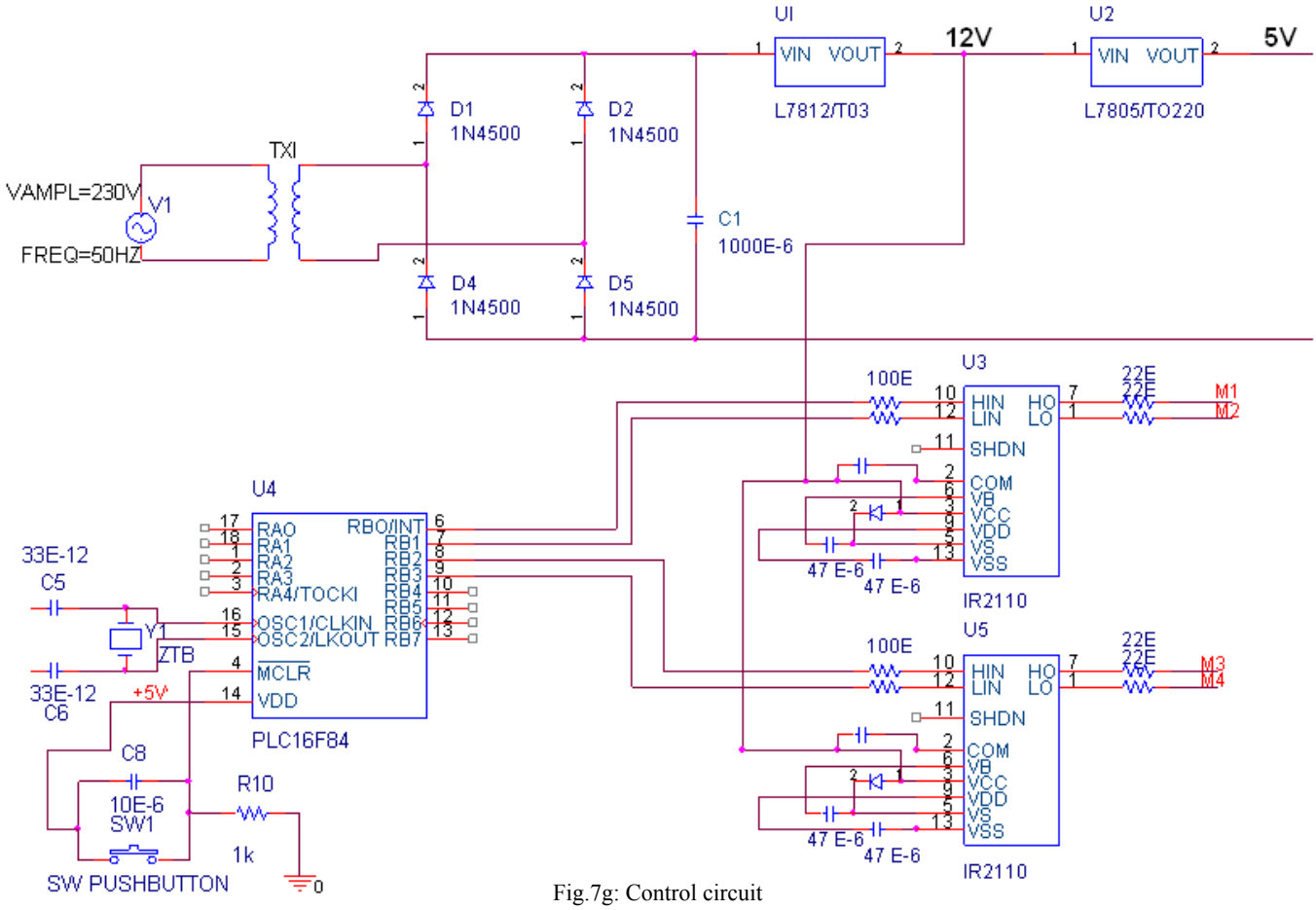
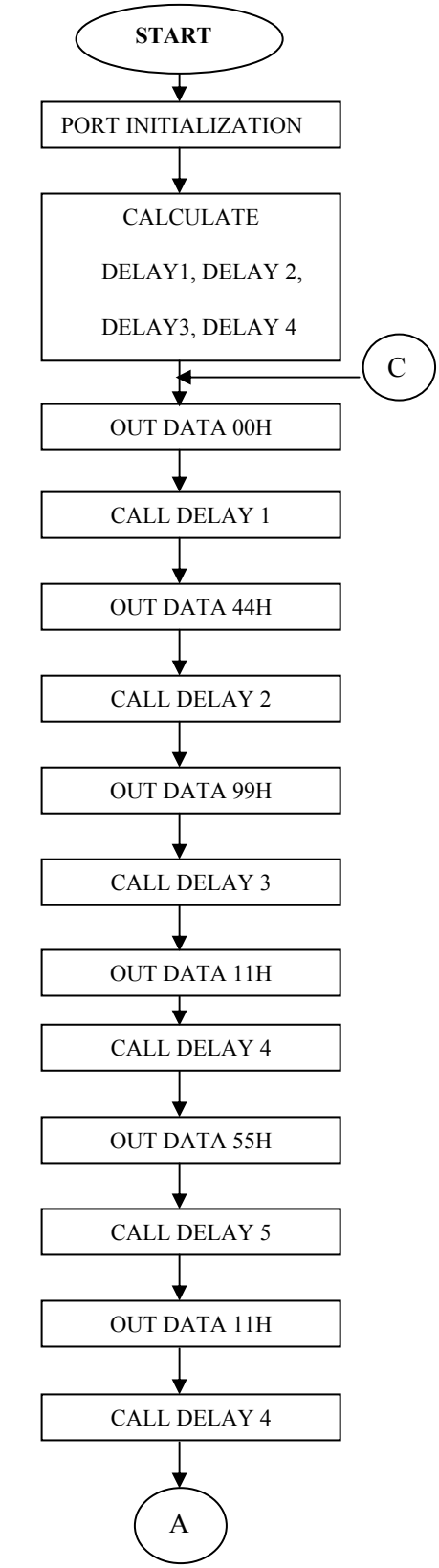
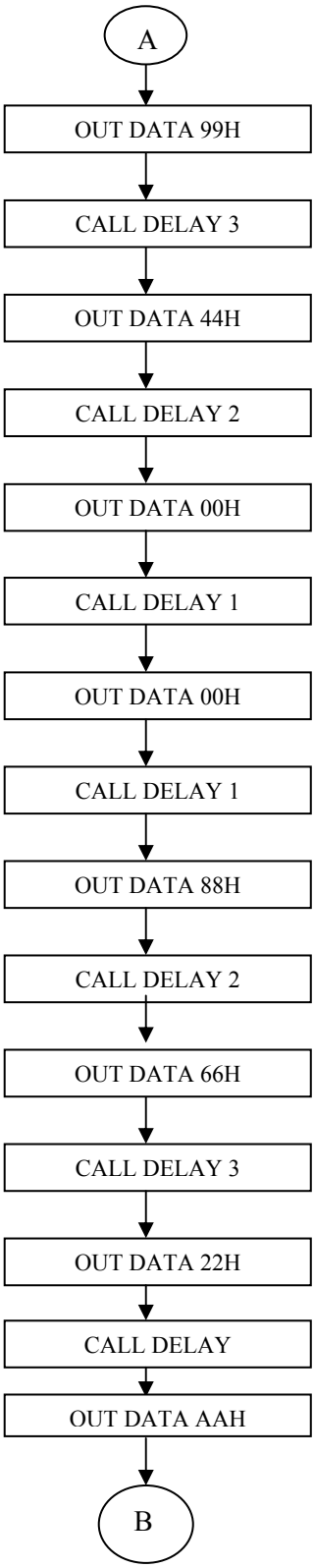


Fig.7g: Control circuit

FLOW CHART





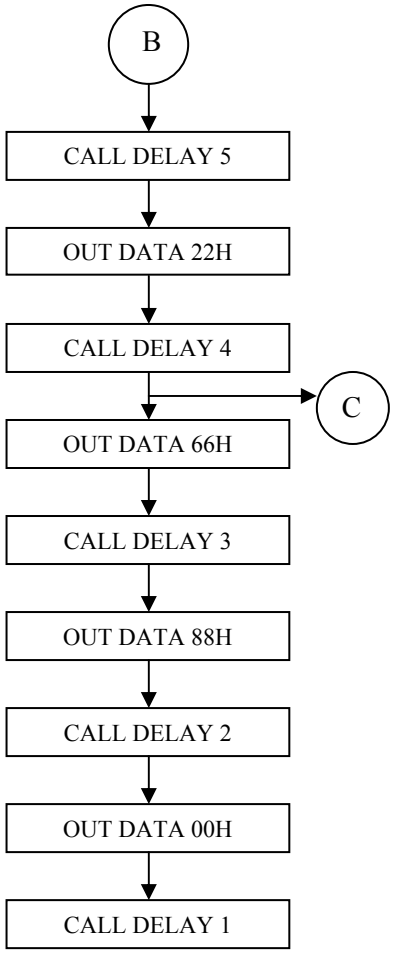


Fig. 7h: Flow chart

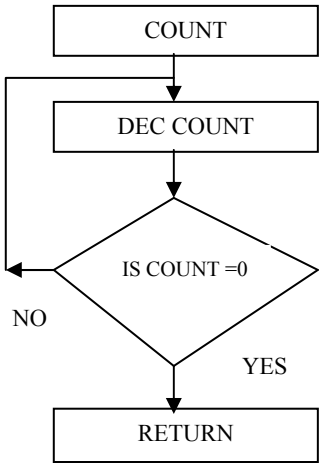


Fig. 7i: Delay Subroutine

V CONCLUSION

Nine-level inverter is proposed for the DVR I the present work. The dynamic voltage restorer is used to improve voltage sags caused by abrupt increase in loads. Multilevel inverters with large number of steps have been used in the DVR system. Multilevel inverter which requires minimum power supplies have been used in DVR system. The DVR can tackle the problem of harmonics caused by non linear loads in manufacturing industries. Other industries can also use DVR to compensate voltage sag. This paper shows simulation and experimental results of nine-level inverter based DVR. THD is found to be much less than that of single PWM inverter. Nine-level inverter is better than other inverters since it inverts voltage of better quality. The experimental results are similar to the simulation results. The nine-level inverter is a viable alternative to the existing inverters to improve the power quality

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BIOGRAPHIES

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Modeling and Control of DSTATCOM with BESS for Mitigation of Flicker

Vasudeo B. Virulkar [1] Mohan V. Aware [2]

Abstract – Industry customers of supply utility such as, electric arc furnaces and arc resistance welder and other such time varying loads which are cyclic in nature are the major flicker source to influence the grid power quality. Distribution STATic Synchronous COMpensator (DSTATCOM) with Battery Energy Storage System (BESS) is proposed as a viable and effective alternative for mitigation of flicker.

This paper examines the dynamic performance of a DSTATCOM coupled with BESS for mitigation of flicker. The detailed modeling of DSTATCOM with BESS and its control strategies are analyzed. The control technique proposed will be focused on the control of energy flow among the system components with effective real power utilization from the batteries. This relives the main power system components from the fluctuating voltages. The detail components of the systems are mathematically modeled to embed the battery energy for the real power utilization to mitigate the voltage fluctuations. Results from digital simulation performed in PSCAD/EMTDC will demonstrate the effectiveness of DSTATCOM/BESS for mitigation of flicker.

Keywords – Battery energy storage (BESS), control techniques, custom power devices, Distribution STATic Synchronous COMpensator (DSTATCOM), Electric Arc Furnace, Flicker

I. INTRODUCTION

Recently, with the growth of industry manufacturers and population, electric power quality becomes more and more important. As one of the most power quality issues, flicker due to feeder voltage fluctuation, influences domestic lighting and sensitive apparatus of nearby transmission and distribution system. Electric arc furnace (EAF), as a major industry customer of supply utility, consumes considerable real power and reactive power with the time-varying, stochastic and even chaotic characteristics during melting and refining process, and therefore generates severe flicker to the grid [1]. There are other industrial applications where high power are switched on and off with a period less than 0.5 s. During the switching on and off of these loads, the demanded high currents determine a voltage drop across the line impedance which is responsible for voltage fluctuations. Voltage fluctuation causes an annoying variation in the output illumination from incandescent or fluorescent lamps. The severity of the annoyance is generally dependent on the frequency and amplitude of the voltage variation and the short circuit capacity of the PCC.

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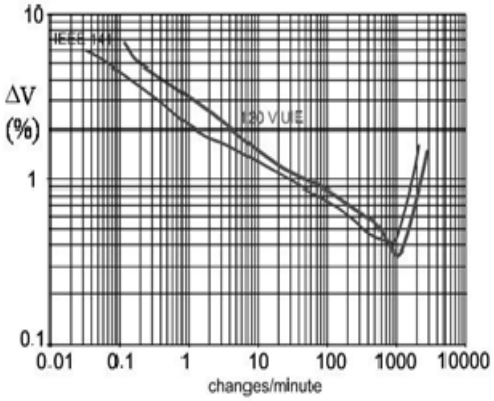

Fig. 1: Maximum permissible voltage fluctuation

It is reported that a small voltage fluctuation of less than 0.5% in the frequency range of 5-10 Hz can cause a visible and uncomfortable incandescent flicker [2]. In addition to the perceptible and sometimes irritating lighting flicker to humans, voltage flicker can also cause electrical equipment efficiency drop, torque and power oscillations, and interference in protection systems. Now a day, consumers require high quality power supply for their sensitive loads. Voltage flicker has therefore been an important power quality concern for Supply utilities, regulatory agencies and customers. To quantify the degree of voltage flicker and its mitigating solutions various definitions and standards have been proposed. The IEEE Standard 1453-2004 [3], which is referred widely, defines maximum permissible voltage flicker levels with respect to frequency as shown in Fig. 1.

Just as flexible as transmission systems (FACTS) controllers are used to improve the quality and reliability of transmission systems, these devices can be used in the distribution system known as custom power devices with significant benefits of bringing the solution to the wide range of problems belonging to the quality and reliability of power that is delivered to the customers [4].
A distribution static compensator or DSTATCOM is a fast response, solid-state power controller that provides flexible voltage control at the point of coupling (PCC) to the utility distribution feeder for mitigations of power quality problem. If it is coupled with energy storage system (ESS), it can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the system voltage. The result is a controlled current flow through the interfacing inductance between DSTATCOM and the distribution system. This enables the DSTATCOM to mitigate voltage fluctuations of the distribution system in instantaneous real-time [5].

This paper discusses the dynamic performance of DSTATCOM with BESS for mitigation of flicker. Modeling and control approaches are proposed, including the detailed modeling of DSTATCOM/BESS device.

Validation of model and control approach is carried out through simulation by using PSCAD/EMTDC.

II. EAF FLICKER MODEL

The Arc furnace operation is a complicated dynamic arcing process. Historically, there are various methods to model arc furnace, such as arcing resistance model, harmonics accumulation model and frequency domain method [6]-[7]. These methods can match the non-linear v-i curve, stochastic and even chaotic characteristics of EAF, therefore, they are satisfactory for the purpose of power quality analysis. However, from the flicker mitigation point of view, a deterministic model needs to be developed.

A. Arc Furnace Model

The arc melting process is a very complicated process, it transfer the electric energy to thermal energy. The random movement of the melting material results in the electrical and thermal dynamics during the arc melting process, thus no two cycles of the arc voltage and current waveforms are identical. By examining the actual V-I characteristic of the arc furnace, in general the arc melting process can be divided into three periods. For convenience of study, some approximations are made according to these three periods, which are explained below.

- In the first period, the arc begins to reignite from extinction. When the arc voltage increases to zero, the arc current also reaches its zero crossing point. As the arc voltage increases to the reignition voltage V_{ig}, the equivalent circuit acts as an open circuit. However, small leakage current exits, which flows throw the floamy slag parallel with the arc. The floamy slag is assumed to be proportional to the arc length.
- In the second period, the arc is established. A transient process appears in the voltage waveform at the beginning of arc melting process. The arc voltage drops suddenly from V_{ig} to a constant value V_d. This process is assumed to be expressed as an exponential function with a time constant τ_1.
- During the third period, the arc begins to extinguish. The arc voltage continues to drop smoothly, except a sharp change after the arc extinction. This process is also assumed to be represented by an exponential function with a time constant τ_2.

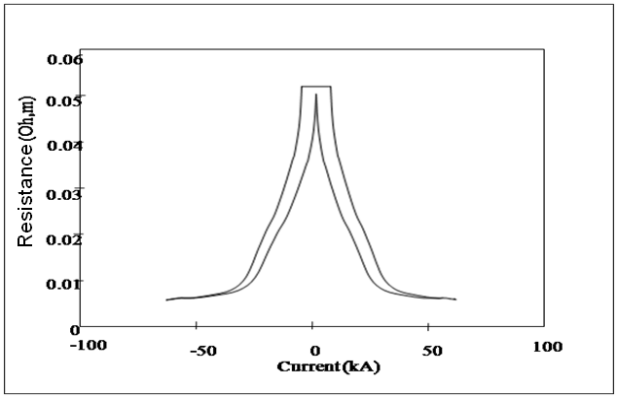

Fig. 2: Current Resistance Curve

Following the above approximation, the arc model can be expressed in the form of current controlled nonlinear resistance as shown in Fig. 2 can be represented by (1)

$$R_a = \begin{cases} R_g & 0 < |i| < i_g \\ & and \ \dfrac{d|i(t)|}{dt} > 0 \\ (V_d + (V_{ig} - V_d) & |i| \geq i_{ig} \\ e^{-(|i|-i_g)/\tau_1}) / |i|; & and \ \dfrac{d|i(t)|}{dt} > 0 \\ \left(V_t + (V_{ig} - v_t)e^{-|i|/\tau_2}\right) & \dfrac{d|i(t)|}{dt} \prec 0 \\ / \left(|i| + i_{ig}\right); & \end{cases} \quad (1)$$

with the continuous condition of the arc resistance at the maximum current value I_{max} and the exponential formulas, some parameters in (1) are calculated as (2);

$$\begin{cases} V_{ig} 1.15 * V_d \\ i_{ig} = \dfrac{V_{ig}}{R_g} \\ Vt = \dfrac{\mathrm{I}_{max} + i_{ig}}{\mathrm{I}_{max}} V_d \end{cases} \quad (2)$$

Normally, the average arc voltage V_d has a linear relationship with the average arc length l, that is,

$$V_d = A + Bl \quad (3)$$

where A and B are constants [8]. Thus, the nonlinear resistance is controlled by the arc length.

As shown in Fig. 3, a flicker model consisting of switching passive loads is proposed to model EAF flicker under worst case condition. This behavior model can represent similar impedance as real-world EAF and therefore produces similar flicker at PCC. From the real-time recorded waveform of EAF, the flicker can be summarized as below: (1) The flicker frequency: around 5Hz; (2) The flicker magnitude *(ΔV/V)*: around 1%; (3) Source *Xs/Rs*; around 3 [9].

Since the 1% flicker is beyond the IEEE irritability threshold curve of IEEE standard [9], the mitigation device has to be applied to mitigate the flicker to an acceptable range. From power flow point of view, the basic principle of flicker mitigation solution can be simply explained as shown in Fig. 4. The power consumed by EAF can be regarded as a constant power (P_0, Q_0) plus a fluctuating power (ΔP, ΔQ).

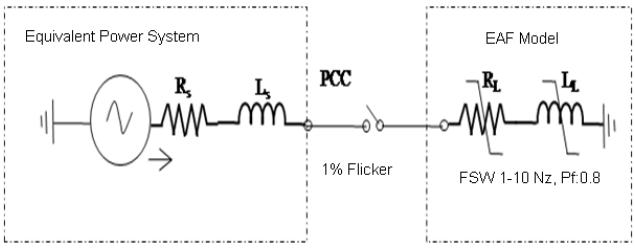

Fig. 3: Worst Case Flicker Model of Electric Arc Furnace

III. FLICKER MITIGATION SOLUTIONS

Generally, P_0 affects the angle stability, load power factor and ΔP is mainly related to the fluctuations of bus voltage magnitude. To solve the EAF power quality issues, ideally,

it is obvious to compensate Q_0, ΔP and ΔQ so that the supply only provides the constant P_0 with unity power factor, and, thereby, the bus voltage magnitude and angle is kept constant.

However, because of cost-effectiveness and other factors, Q_0, ΔP and ΔQ cannot be fully compensated, but only mitigated to an acceptable level in the real world. Particularly, ΔP mainly affects the voltage angle other than flicker and requires energy storage source for compensation. Flicker Mitigation techniques can be classified into three types: (1) Passive filters, which can be either series or shunt [11].
The passive filters are simple, reliable, low-cost and highly efficient, it is difficult to design for a stiff system, time consuming for tuning, easy to induce resonance, and not, susceptible to system impedance variations. (2) Series active compensators, such as series impedance regulation [12].

Although, increasing series reactance mitigates the flicker to some extent, it results in voltage reduction and consequently EAF productivity. Moreover, it is also expensive and cumbersome to control the upstream transformer reactance in today's deregulated power system. (3) Shunt active compensator, such as SVC and STATCOM. SVC can improve the power quality and increase the EAF productivity leading to additional economic benefits. However, it cannot react to the fast varying flicker (1Hz-20Hz) very well within the inherent limit of relatively low bandwidth and its dynamic performance for flicker mitigation is limited. The state-of-art solution is the DSTATCOM based on high frequency switching voltage source converter (VSC). While SVC performs as controlled reactance admittance, DSTATCOM functions as synchronous voltage source. The DSTATCOM response time is less than one cycle and follows the fast changing flicker well [13].

IV. Modeling of the DSTATCOM/BESS

A. Modeling of DSTATCOM

A DSTATCOM consists of three-phase six pulse voltage source inverter (VSI) shunt connected to the distribution network by means of coupling transformer with the ability to both generate and absorb reactive and active power.

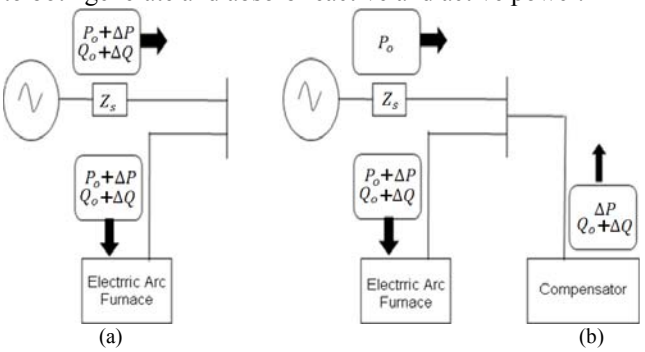

Fig. 4: Electric Arc Furnace (a) without compensator (b) With compensator

The reactive power exchange between the AC system and the DSTATCOM is controlled varying the magnitude of the fundamental component of the inverter voltage above and below that of AC system; this is achieved by small variations in the switching angle of the semiconductor devices. When the voltage's fundamental component produced by the inverter is forced to lag or lead the AC system voltage by a few degrees, an active power may flow into or out of the inverter modifying the DC capacitor voltage value. Otherwise, if the inverter supplies only reactive power, the active power provided by the capacitor is zero, therefore the DC capacitor does not modify its voltage.

The schematic diagram of a voltage source converter is shown in Fig. 5.
The ac source voltages are e_a,e_b,and e_c. The ac currents are i_a, i_b, and i_c. The ac terminal voltages of the converter are v_a, v_b, and v_c. The dc voltage and current are V_{dc} and I_{dc}, respectively.

The ac side impedance is modeled as an inductor L in series with a resistor R. The dc side capacitor is C_{dc}. And the dc load is R_{dc}. The converter is controlled under sinusoidal PWM technique. The modulation signal of phases a, b, and c are m_a, m_b, and m_c, respectively. The relationship between the fundamental components of the ac terminal voltages v_a, v_b, v_c, and the dc voltage V_{dc} is

$$v_a = \frac{1}{2} m_a V_{dc}; \quad v_b = \frac{1}{2} m_b V_{dc}; \quad v_c = \frac{1}{2} m_c V_{dc}; \tag{4}$$

Taking the ac source voltage as the reference phasor, the conventional dynamic equation in d-q coordinates are

$$\frac{d}{dt} V_{dc} = -\frac{1}{R_{dc} C_{dc}} V_{dc} + \frac{3}{2C_{dc}} M_d I_d \tag{5}$$

$$\frac{d}{dt} I_d = -\frac{R}{L} I_d + \omega I_q - \frac{1}{2L} M_d V_{dc} + \frac{1}{L} E_d \tag{6}$$

$$\frac{d}{dt} I_q = -\omega I_d - \frac{R}{L} I_q - \frac{1}{2L} M_q V_{dc} \tag{7}$$

Where V_{dc}, I_d, and I_q are the state variables, M_d, and M_q are the inputs, and V_{dc} and I_q are outputs, and E_d is a constant.
Obviously, (5)-(7) represents a nonlinear system and it is not easy to design a controller for such a system. However, the above system can be modified to a linear system through a set of non-linear transformations. The power consumed on the dc-side can be expressed as

$$P_{dc} = V_{dc} C_{dc} \frac{d}{dt} V_{dc} + \frac{V_{dc}^2}{R_{dc}} \tag{8}$$

The power delivered from the ac side can be written as

$$P_{ac} = \frac{3}{2} E_d I_d \tag{9}$$

The power delivered from the ac side can be written as

$$P_{ac} = \frac{3}{2} E_d I_d \tag{10}$$

If the ac side resistor R is very small, the power loss in R can be neglected. In most applications, this assumption is valid. Therefore, from (8) and (9)

If (V_{dc}^2) is taken as a dynamic equation instead of (5). As a result, the original nonlinear system can now be written as

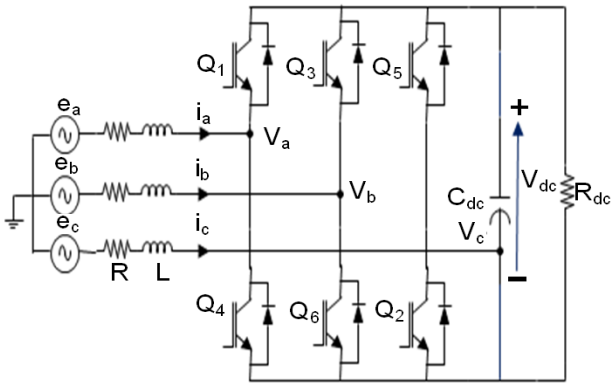

Fig. 5: Schematic Diagram of a Voltage Source Converter

$$\frac{d}{dt}\left(V_{dc}^2\right) = -\frac{2}{R_{dc}C_{dc}}\left(V_{dc}^2\right) + \frac{3E_d}{C_{dc}}I_d \tag{11}$$

$$V_{dc}C_{dc}\frac{d}{dt}V_{dc} + \frac{V_{dc}^2}{R_{dc}} = \frac{3}{2}E_dI_d \tag{12}$$

$$\frac{d}{dt}I_d = -\frac{R}{L}I_d + \omega I_q - \frac{1}{L}E_d \tag{13}$$

$$\frac{d}{dt}I_q = -\omega I_d - \frac{R}{L}I_q - \frac{1}{L}V_q \tag{14}$$

where $V_d = (1/2)M_dV_{dc}$ and $V_q = (1/2)M_qV_{dc}$ are the new inputs of the system. Equations (12) - (14) represent a linear model that describes the DSTATCOM.

In general, the DSTATCOM can be utilized for providing voltage regulation, power factor correction, harmonics compensation and load leveling [14]. The addition of energy storage through an appropriate interface to the custom power leads to more flexible integrated controller. The ability of the DSTATCOM/ESS of supplying effectively extra active power allows expanding its compensating actions, reducing distribution losses and enhancing the operation of the grid [15].

The presented VSI corresponds to a dc to ac switching power inverter using insulated Gate Bipolar Transistors (IGBT). In the distribution voltage level, the switching device is generally the IGBT due to its lower switching losses and reduced size. In addition, the rating of custom power devices is relatively low.
As a result the voltage control of DSTATCOM can be achieved by using high power fast-switched IGBTs. This topology supports the future use of PWM control even for high power applications.

The connection to the utility grid is made by using low pass sine wave filters in order to reduce the perturbation on the distribution system from high-frequency switching harmonics generated by PWM control. The total harmonic distortion (THD) of the output voltage of the inverter combined with sine wave filter is less than 5% at full rated unity power factor load. Typically, leakage inductance of the set up transformer windings is high enough as to build the sine wave filter simply by adding a bank of capacitors in the PCC. In this way, an effective filter is obtained at low cost, permitting to improve the quality of the voltage waveforms introduced by the PWM control to the power utility and meeting the power quality requirement [10].

A simplified scheme of the DSTATCOM/BESS equivalent circuit is shown in Fig. 6. The DSTATCOM is considered as a voltage source that shunt connected to the distribution network through inductance L_s, accounting for the equivalent leakage reactance of the set-up coupling transformer and the series resistance R_s, representing the transformer winding resistance and VSI semiconductor conduction losses. The mutual inductance M represents the equivalent magnetizing impedance of the set-up transformers. In the dc side, the capacitance of the dc bus capacitor is described by C_d whereas
the switching losses of the VSI and power loss in the capacitors are considered by R_p.
The dynamic equations governing the instantaneous values of the three-phase output voltage in the ac side of the DSTATCOM and the current exchanged with the distribution grid are given by (13) and (14).

$$\begin{bmatrix} v_{inv_a} \\ v_{inv_b} \\ v_{inv_c} \end{bmatrix} - \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \left(R_s + sL_s\right)\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{15}$$

where:

$$s = \frac{d}{dt}, R_s = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix}, L_s = \begin{bmatrix} L_s & M & M \\ M & L_s & M \\ M & M & L_s \end{bmatrix} \tag{16}$$

Under the assumption that the system has no zero sequence components, all currents and voltages can be uniquely transformed into the synchronously-rotating *dq* reference frame. Thus, the new coordinate system is defined with the *d*-axis always coincident with the instantaneous reactive power.
By applying Park's transformation [16] (15) and (16) can be transformed into *dq* reference frame as follows:

$$\begin{bmatrix} v_{inv_d} - v_d \\ v_{inv_q} - v_q \\ v_{inv_0} - v_0 \end{bmatrix} = K_s\begin{bmatrix} v_{inv_a} - v_a \\ v_{invb_a} - v_b \\ v_{invc_a} - v_c \end{bmatrix}, \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = K_s\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{17}$$

where K_s is Park's transformation matrix given by

$$K_s = \sqrt{\frac{2}{3}}_s\begin{bmatrix} \cos\theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin\theta & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{18}$$

then by neglecting the zero sequence components, (19) and (20) are derived.

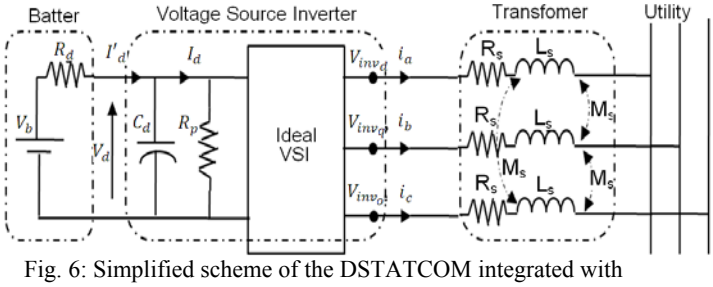

Fig. 6: Simplified scheme of the DSTATCOM integrated with BESS

$$\begin{bmatrix} v_{inv_d} \\ v_{inv} \end{bmatrix} - \begin{bmatrix} v_d \\ v_q \end{bmatrix} = (R_s + sL_s)\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} -\omega & 0 \\ 0 & \omega \end{bmatrix}L_s'\begin{bmatrix} i_d \\ i_q \end{bmatrix}, \tag{19}$$

Where:

$$R_s = \begin{bmatrix} R_s & 0 \\ 0 & R_s \end{bmatrix}, L_s' = \begin{bmatrix} L_s' & 0 \\ 0 & L_s' \end{bmatrix} = \begin{bmatrix} L_s - M & 0 \\ 0 & L_s - M \end{bmatrix} \tag{20}$$

B. Modeling of BESS

Various types of energy storage technologies can be incorporated into the dc bus of the DSTATCOM, namely superconducting magnetic energy storage (SMES), supercapacitores (SC), flywheel and battery energy storage system (BESS), among others. However, lead acid id batteries offer a more economical solution for application in the mitigation of flicker that require small devices for supplying power for small period of time and intermittently. The energy stored in a lead acid battery is chemical energy that is translated into electrical energy. Lead acid batteries are rechargeable and have the following reversible reaction: [17]

$$Pb + PbO_2 + 2H_2SO_4 \leftrightarrow 2PbSO_4 + 2H_2O \tag{21}$$

The battery voltage is related to the sum of the reduction and oxidation potentials. Electrical energy is produced when the chemicals in the battery react with the following conditions:

- State of charge
- Battery storage capacity
- Rate of charge/discharge
- Environmental temperature
- Age/Shell life

The battery model can be represented by an equivalent electric network as shown in Fig. 7 along with the dynamic equations representing the charge storage process and electrolyte heating

$$Q_e = \int_0^t -\mathrm{I_m}(\tau)d\tau \tag{22}$$

$$C_\theta \frac{d\theta}{dt} = \frac{\theta - \theta_e}{R_\theta} + P_s \tag{23}$$

Where:

Q_e so-called "extracted charge," i.e., the charge that has been actually extracted from the battery starting from the battery completely full (battery full when t=0);

C_θ and R_θ battery thermal capacitance and resistance, respectively;

P_s Heating power generated inside the battery by conversion from electrical or chemical energy.

It has to be remembered that the resistance R_k and capacitance C_k shown in Fig. 6 are function of the battery state-of-charge and electrolyte temperature.

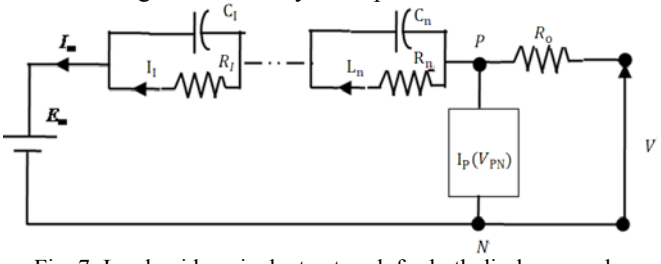

Fig. 7: Lead-acid equivalent network for both discharge and charge

The BESS as shown in Fig. 5 is represented by an ideal dc voltage source V_b and a series resistance R_b, accounting for battery internal resistance. The self-discharge and leakage as well as capacity of the batteries are represented by parallel combination of resistance and capacitor.

The DSTATCOM ac and dc sides are related by the power balance between the input and the output on an instantaneous basis as described by (24) and (25).

$$P_{ac} = P_{dc} \tag{24}$$

$$\frac{3}{2}\left(v_{inv_d} i_d + v_{inv_q} i_q\right) = \left(\frac{V_b - V_d}{R_d}\right) - C_d V_d \frac{dV_d}{dt} - \frac{V_d^2}{R_p} \tag{25}$$

The VSI of the DSTATCOM basically generates the ac voltage (v_{inv}) from the dc voltage (V_d). Thus, the onnection between the dc-side voltage and the generated ac voltage can be described by using the average witching function matrix S and the factor k_{inv} as given by (26) through (27).

$$\begin{bmatrix} v_{inv_d} \\ v_{inv_q} \end{bmatrix} = k_{inv} \begin{bmatrix} S_d \\ S_q \end{bmatrix} V_d, \tag{26}$$

with the factor:

$$k_{inv} = \frac{1}{2} ma \tag{27}$$

Being,

m: modulation index, $m \in [0, \quad 1]$,

$a = \frac{n_2}{n_1}$: voltage ratio of the coupling set-up transformer

And the average switching factor matrix for dq reference frame,

$$\begin{bmatrix} S_d \\ S_q \end{bmatrix} = \begin{bmatrix} \cos\alpha \\ \sin\alpha \end{bmatrix}, \tag{28}$$

with:

α: phase-shift of the converter output voltage from the reference position

Essentially, (16), (17) and (24) through (27) can be summarized in the state-space as follows.

$$s\begin{bmatrix} i_d \\ i_q \\ V_d \end{bmatrix} = \begin{bmatrix} \frac{-R_s}{L_s'} & \omega & \frac{k_{inv} S_d}{L_s'} \\ -\omega & \frac{-R_s}{L_s'} & \frac{k_{inv} S_q}{L_s'} \\ \frac{3}{C_d} k_{inv} S_d & \frac{3}{C_d} k_{inv} S_q & \frac{2}{C_d}\left(\frac{R_b R_p}{R_b + R_p}\right) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ V_d \end{bmatrix} + \begin{bmatrix} \frac{|v|}{L_s'} \\ 0 \\ \frac{2}{R_b C_d} V_b \end{bmatrix} \tag{29}$$

IV. CONTROL STRATEGY

The operation of the DSTATCOM/BESS as a flicker mitigating component is achieved by a suitable control algorithm that manages the energy transfer among the BESS, dc-link capacitor, and the distribution system. The analysis of the energy control system (ECS) is based on the following assumptions. The control systems of the converter are able to keep the source power P_s and the BESS power P_{BESS} close to their reference, i.e. P_s^* and P_{BESS}^*;

Losses in the passive components such as inductors, capacitors, storage device, and in the static switches are neglected

These two assumptions are acceptable because of the low time response of the control system used to drive the converter and the small amount of the losses in the passive components. Furthermore, the time constant of the storage device must be low enough to allow the tracking of the energy variations demanded by the ECS. The analysis of

the ECS can be usefully carried out in terms of power flow and energy balance using the Laplacian notation [19]. The proposed control algorithm is shown scheme of Fig. 8. In this scheme the input control variables of the DSTATCOM/BESS are the energy in the dc-link capacitor E_C^* and the energy in the BESS E_{BESS}^*.

The controller R_1 generates the reference source power, which combined to the load power gives the reference DSTATCOM power. This has to be injected by the VSI into the PCC. At the same time, the controller R_2 generates the firing signals for the dc/dc chopper, which controls the power flowing into the storage device. The controller $R_3(s)$ varies the energy reference in the BESS on the basis of the error of the dc capacitor energy. Once the parameters of the controller R_1, R_2, and R_3 are defined, it is possible to determine the transfer function of the control loops represented in Fig. 9. The control algorithm has been designed to manage the transfer of energy between the BESS and the dc-link capacitor during the transient conditions caused by the load variations. In this way the ECS operates in order to recover the energy level in the capacitor, using a fraction of the energy stored in the BESS. During load changes, the energy variations in the capacitor are quickly compensated by the energy transfer between the BESS and the dc-link capacitor. Consequently, the energy required by the load can be considered as coming directly from the BESS. The source is not required to supply the full load power, but an increasing amount of power. The use of BESS to smooth the load variation is necessary because the dc link capacitor has very small amount of energy stored. Moreover, its energy variation must be minimized for correct operation of VSI with practically constant dc-link voltage.

Assuming the capacitor energy and the BESS energy are close to their references, respectively E_C^* and E_{BESS}^*, an increase of the load power P_L determines a power flow from the capacitor to the ac side, yielding an error $\Delta E_C = E_C^* - E_C$ in the capacitor stored energy.

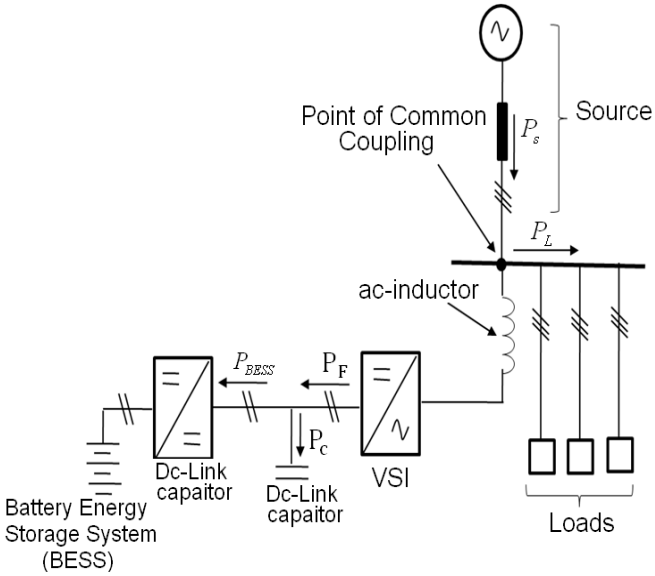

Fig. 8: Scheme of DSTATCOM/BESS System

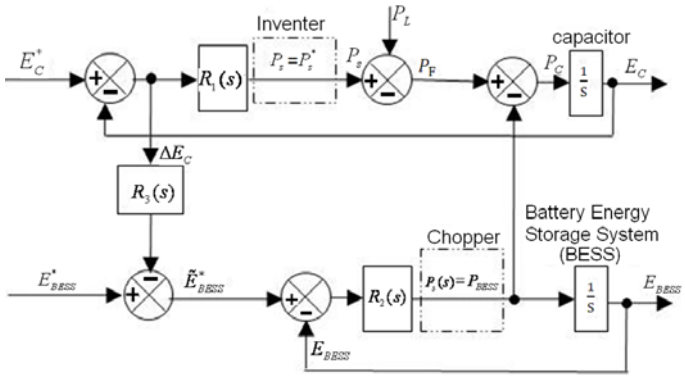

Fig. 9: Energy Control System

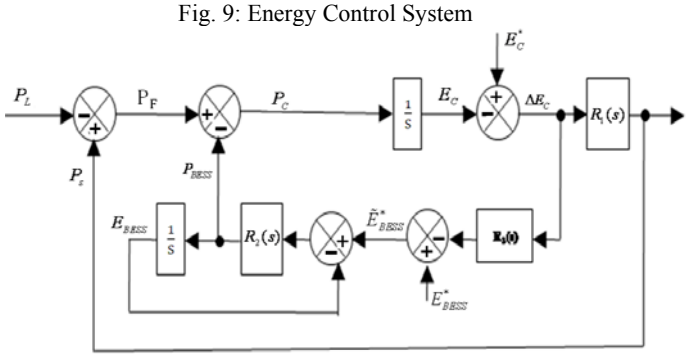

Fig. 10: Block Diagram showing the relationship between P_L and P_s

Assuming a simple proportional controller the new BESS energy reference will be given by:

$$\tilde{E}_{BESS}^* = E_{BESS}^* - K_{P3}\Delta E_C \tag{29}$$

This new lower value of the reference allows the chopper to recover the dc-link voltage using the energy stored in BESS.

A scheme shown in Fig. 8 is used to analyze the operation of DSTATCOM/BESS for mitigation of flicker due to pulsating loads. Analyzing the transfer function of the control loop given in Fig. 9 , the DSTATCOM/BESS can smooth the source power variation due to pulsating loads. The control scheme of Fig. 10 is derived from the basic scheme of Fig. 9 by considering the load power P_L as input signal, and the source power P_s as output variable.

The reference for the dc-link capacitor energy and for the BESS energy can be considered as disturbances having constant values. The relationship between the source power and the load power can be easily calculated assuming the controller of Fig. 3 with following expressions:

Capacitor energy controller:

$$R_1(s) = K_{P1} + \frac{K_{I1}}{s}$$

BESS energy controller:

$$R_2(s) = K_{P2}$$

BESS energy reference controller:

$$R_3(s) = K_{P3,}$$

With these assumptions the expression for $P_s(s)$ is given by the sum of three terms as represented in (17) and in Fig. 10.

$$P_s(s) = G_C(s)E_C^* + G_{BESS}(s)E_{BESS}^* + G_L(s)P_L \tag{30}$$

The expressions for $G_C(s), G_{BESS}(s), G_L(s)$ are given in Appendix. Under the assumption that E_C^* and E_{BESS}^* are constant, by applying final value theorem to the step response of the transfer function $G_L(s), G_{BESS}(s)$ yields

$$\begin{cases} \lim_{s\to 0} s\dfrac{1}{s} G_C(s) = 0 \\ \lim_{s\to 0} s\dfrac{1}{s} G_{BESS}(s) = 0 \end{cases} \quad (31)$$

This means that the relationship between the BESS power and the load power is given only by the transfer function $G_L(s)$. On the basis of this result, the analysis of the control system can be carried out with reference to the following open loop transfer function derived from $G_L(s)$,

$$G_{La}(s) = \frac{(K_{P1}s + K_{1I})(s + K_{P2})}{s^2(s + K_{P3}K_{P2})} \quad (32)$$

The resulting control system can be simplified as represented in Fig. 11. The parameters of the transfer function (32) must be tuned to obtain the desired behavior of the source power in response to the load power variation. A deep discharge of the BESS determines a greater amount of energy flowing from the DSTATCOM/BESS towards PCC, yielding to a longer time interval during which the DSTATCOM/BESS supplies the load power.

V. DIGITAL SIMULATION

For a 100 MVA Electric Arc Furnace connected to system of 34.5/0.9 kV is simulated in PSCAD/EMTDC with the 50 MVA DSTATCOM and 10 MW/10 s VRLA batteries to validate the proposed modeling and control strategy. The Flicker meter simulated in the PSCAD/EMTD is used to measure the short term flicker severity index P_{st}. The values of P_{st} obtained without compensator and with compensator are shown in Table-1. Fig. 13 through 16 shows the real power and reactive power from the source before compensation and after compensator DSTATCOM coupled with BESS and not coupled with BESS. The Short Time flicker severity index (Pst) for three different cases are s shown in Table-I.

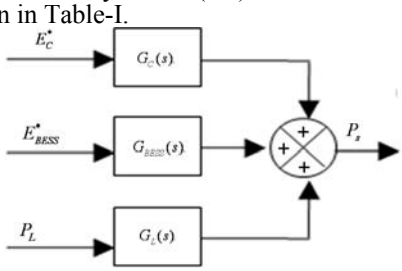

Fig. 11: Simplified block diagram

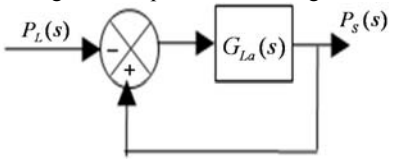

Fig. 12: Source power regulation loop

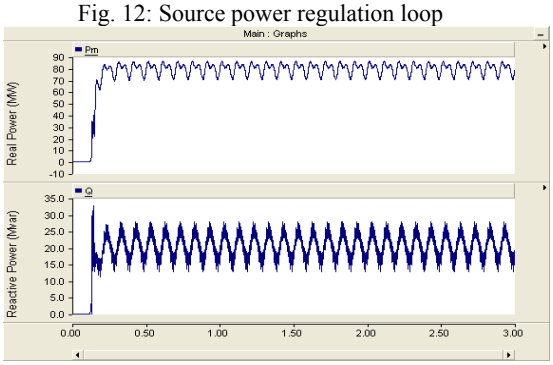

Fig. 13: Real Power and Reactive Power from Source without Compensation

Table 1: Flicker severity index

Compensation strategy	Pst
No compensation means	5.6
Compensation with DSTATCOM without BESS	1.35
Compensation with DSTATCOM with BESS	0.78

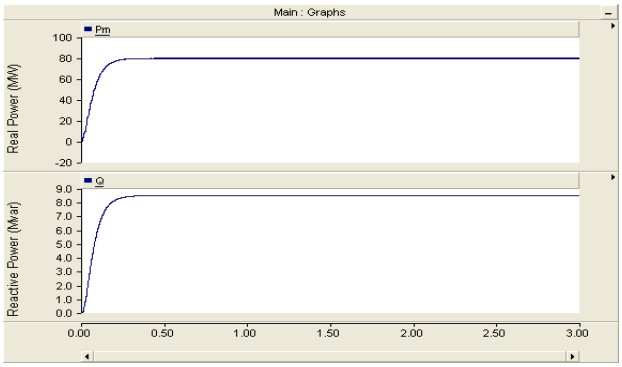

Fig. 14: Real Power and Reactive Power from Source with DSTATCOM and BESS

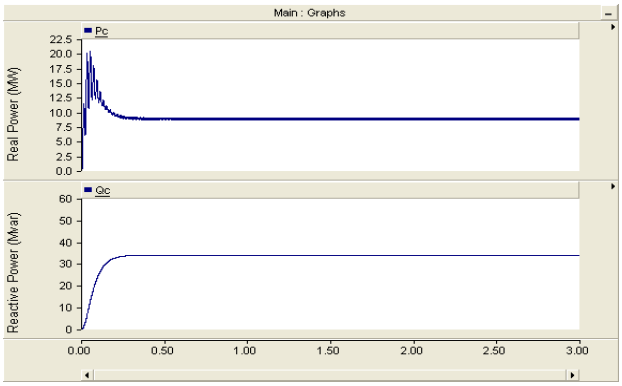

Fig. 15: Real Power and Reactive Power from Source with DSTATCOM and BESS

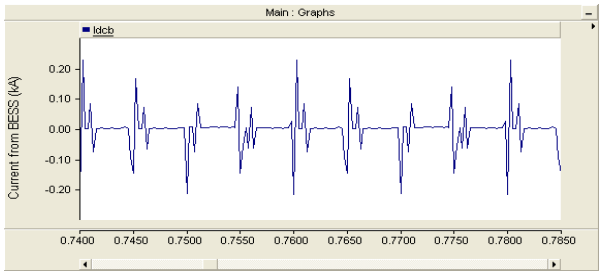

Fig. 16: Current from BESS

VI. CONCLUSION

The paper describes mitigation of flicker due to electric arc furnace by means of DSTATCOM with Battery Energy Storage System (BESS).

In the investigations performed here, the flicker, as indicated by the P_{st} value of the PCC voltage, was initially 5.6 without compensation. The system with DSTATCOM (without BESS) Pst equals to 1.35, indicating the reduction of flicker by 75 % and with DSTATCOM and BESS Pst is 0.78 indicating the reduction in flicker nearly negligible and inconformity with IEEE 1453. It indicates that mitigation of flicker with DSTATCOM and BESS is more effective than DSTATCOM alone by supporting the active and reactive power at the same time. In this paper, the

authors presented the modeling and control strategy of the DSTATCOM/BESS for mitigation of voltage flicker.

APPENDIX

$$G_C(s)=\frac{K_{P1}s^3+\left(K_{P1}K_{P2}+K_{I1}\right)s^2+K_{P1}K_{P2}s}{s^3+\left(K_{P1}+K_{P2}+K_{P3}K_{P2}\right)s^2+\left(K_{I1}+K_{P1}K_{P2}\right)s+K_{P1}K_{P2}} \quad \text{(A1)}$$

$$G_{BESSC}(s)=\frac{K_{P1}K_{P2}s^2+K_{P1}K_{P2}s}{s^{32}+\left(K_{P1}+K_{P2}+K_{P3}K_{P2}\right)s^2+\left(K_{I1}+K_{P1}K_{P2}\right)s+K_{P1}K_{P2}} \quad \text{(A2)}$$

$$G_L(s)=\frac{K_{P1}s^2+\left(K_{P1}K_{P2}+K_{I1}\right)s+K_{I1}K_{P2}}{s^{32}+\left(K_{P1}+K_{P2}+K_{P3}K_{P2}\right)s^2+\left(K_{I1}+K_{P1}K_{P2}\right)s+K_{P1}K_{P2}} \quad \text{(A3)}$$

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BIOGRAPHIES

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Single-Phase SEPIC Based PFC Converter for PMBLDCM Drive in Air-Conditioning System

Sanjeev Singh[1] Bhim Singh[2]

Abstract – In this paper, a permanent magnet brushless DC motor (PMBLDCM) is employed in air-conditioning systems and operated at rated torque and variable speed to achieve energy conservation. A single-phase single-switch power factor correction (PFC) based single ended primary inductor converter (SEPIC) is used to regulate DC bus voltage of voltage source inverter (VSI) to feed PMBLDCM. The analysis, design and performance evaluation of the proposed PFC converter is carried out for a 1.2 kW, 1200 rpm, 164 V PMBLDCM used in air-conditioning system. The proposed PFC converter is modeled and its performance is simulated in Matlab-Simulink environment. An exhaustive evaluation of its performance is carried out to demonstrate improved power factor in wide range of speed of the drive and AC input voltage.

Keywords – PFC converter, SEPIC, PMBLDC motor, air-conditioning, power quality (PQ)

I. Introduction

Air-conditioners (Air-Cons) constitute a considerable amount of load in AC distribution system [1]. However, most of the existing air-conditioners are not energy efficient and thereby, provide a scope for energy conservation. Air-Cons in domestic sector are usually driven by a single-phase induction motor running at constant rated torque with on-off control [1]. A permanent magnet brushless DC motor (PMBLDCM) is a good drive for Air-Cons due to its high efficiency, silent operation, compact size, high reliability, ease of control and low maintenance requirements.

A PMBLDCM is a kind of three-phase synchronous motor having permanent magnets on the rotor [2-7]. Usually these PMBLDCMs in small Air-Cons are powered from single-phase AC mains through a diode bridge rectifier (DBR) with smoothening DC capacitor and a three-phase voltage source inverter (VSI) [3-4, 6-7]. Because of uncontrolled charging of DC link capacitor, the AC mains current waveform is a pulsed waveform featuring a peak value higher than the amplitude of the fundamental input current as shown in Fig. 1. The power factor (PF) is 0.741 and crest factor (CF) of AC mains current is 2.2 with 67% efficiency of the drive. Therefore, many power quality (PQ) problems arise at input AC mains including poor power factor, increased total harmonic distortion (THD) and high crest factor (CF) of AC mains current etc. These PQ problems as addressed in IEC 61000-3-2 [8] especially in low power appliances become severe for the utility when many such drives are employed simultaneously at nearby locations.

Therefore, PMBLDCM drives having inherent power factor correction (PFC) become the preferred choice for the Air-Cons. The PFC converter draws sinusoidal current from AC mains in phase with its voltage. In this PFC converter a DC-DC converter topology is mostly used amongst several available topologies [9-16] e.g. boost, buck-boost, Cuk, SEPIC, zeta converters with variations of capacitive/inductive energy transfer. It results in an improved performance, such as reduction of AC mains current harmonics, acoustic noise, electromagnetic interference (EMI) and number of components; improved efficiency, wide input voltage range utilization etc.

Some attempts [11,13,16] have been made to introduce PFC feature in PMBLDCM drives using uni-polar excitation [13] and bipolar excitation [11,16] of PMBLDCMs. For automotive air-conditioning a low voltage PMBLDCM drive has been reported [15] with compact size of the complete system. PMBLDCM with boost PFC converter [11] and PMSM with improved power quality converter [12] have been reported for domestic Air-Cons. However, a PMBLDCM is best suited for air-conditioning system due to simple control and its high average torque.

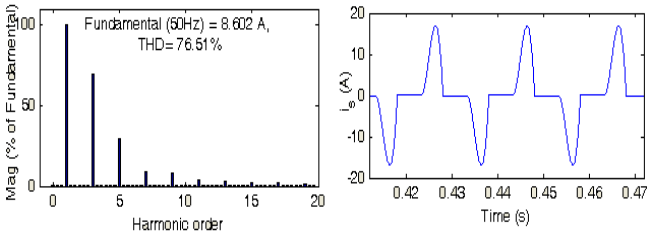

Fig. 1: Supply current and harmonic spectrum (at 220 V_{AC}) of a DBR fed PMBLDCM drive at rated load.

A single ended primary inductor converter (SEPIC), as a PFC converter, inherits merits of continuous input current, ripple current reduction [16-17]. Therefore, a SEPIC converter is proposed for PFC in a PMBLDCM drive used to drive Air-Cons. This paper, deals with detailed design and exhaustive performance evaluation of the SEPIC converter as a PFC converter, for PMBLDCM driven air-conditioner system.

II. Operation and Control of SEPIC Converter Fed PMBLDCM

Fig. 2 shows the proposed SEPIC based PFC converter fed PMBLDCM drive for the speed control as well as PFC in wide range of input AC voltage. A proportional-integral (PI) controller [4] is used for the speed control of the PMBLDCM driving constant torque compressor of Air-Con. The speed signal converted from the rotor position of PMBLDCM (sensed using Hall effect sensors) are compared with the reference speed. The resultant speed error is fed to a speed controller to give the torque which is converted to current signal. This signal is multiplied with a rectangular unit template in phase with top flat portion of motor's back EMF to get reference currents of the motor.

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These reference motor currents are compared with sensed motor currents to give current error. These current errors are amplified and compared with triangular carrier wave to generate the PWM pulses for VSI switches.

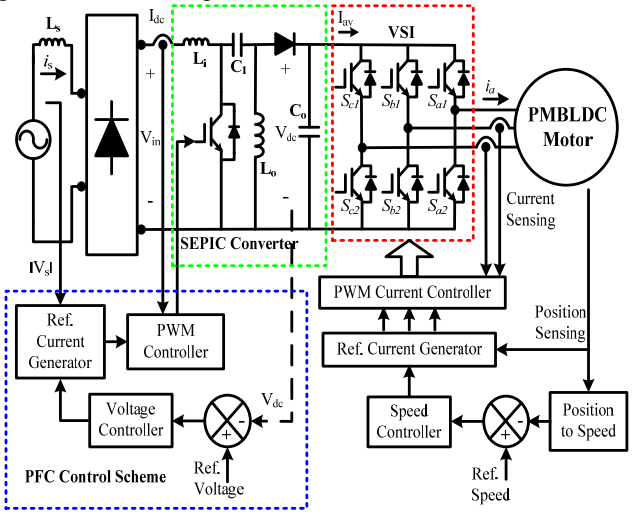


Fig. 2: Control Schematic of PFC based SEPIC Converter fed PMBLDCM Drive

The SEPIC based PFC converter has a conventional DBR fed from single-phase AC mains followed by the SEPIC DC-DC converter, an output ripple filter and a three-phase VSI to feed the PMBLDC motor. The DC-DC converter provides a controlled DC voltage from uncontrolled DC output of DBR, with PFC action through high frequency switching. The duty ratio (D) of the DC-DC converter is controlled by the DC voltages at its input and output. The switching frequency (f_s) is decided by the switching device used, power range and switching losses of the device. In this work, insulated gate bipolar transistors (IGBTs) are used as the switching devices in the PFC switch as well as in VSI bridge, because IGBTs can operate in wide switching frequency range to make optimum balance between magnetics, size of filter components and switching losses.

The PFC controller has outer voltage control loop and inner current control loop. An average current control scheme with current multiplier approach is used in this topology and a continuous conduction mode (CCM) operation of SEPIC is considered for PMBLDCM drive. The voltage control loop starts with sensing of DC link voltage which is compared with the reference DC link voltage. The error DC voltage is passed through a voltage PI controller to give the modulating current signal. This signal is multiplied with a unit template of input AC voltage and the resultant signal is compared with DC current sensed after the DBR to give current error. This current error is amplified and amplified signal is then compared with saw-tooth carrier wave to generate the PWM switching pulses for the DC-DC converter switch.

III. Design of SEPIC PFC Converter for PMBLDCM

Fig. 2 shows the proposed SEPIC converter fed PMBLDCM drive. The SEPIC converter achieves high power density and fast transient response when operated at high switching frequency [16]. It is designed for constant current in the intermediate inductor (L_o) as it operates on the principle of an inductive energy transfer [17]. The boost inductor (L_i), and capacitors (C_1, C_o) are designed according to maximum allowable current and voltage ripple during transient conditions of the PMBLDCM drive. The design equations governing the duty ratio and other component values are as follows.

Output voltage	$V_{dc}=D\,V_{in}/(1-D)$	(1)
Boost inductor	$L_i= D\,V_{in}/\{f_s\,(\Delta I_{Li})\}$	(2)
Intermediate capacitor	$C_1= D\,/\,\{(Rf_s)\,(\Delta\,V_{C1}/\,V_o)\}$	(3)
Output filter inductor	$L_o= (1-D)V_{dc}/\{f_s(\Delta I_{Lo})$	(4)
Output filter capacitor	$C_o=I_{av}/(2\omega\Delta V_{dc})$	(5)

The PFC converter is designed for a constant DC link voltage V_{dc} = 400V at V_{in} = 198V for V_s = 220V. Other design data are f_s = 40kHz, I_{av} = 5A, R= 80Ω, ΔI_{Li}= 0.75A, ΔI_{Lo}= 0.75 A (15% of I_{av}), ΔV_{dc}= 5V (1.25% of V_{dc}), ΔV_{C1}= 15V (3.75% of V_{dc}). The design parameters calculated are L_i=4.5mH, C_1=5µF, L_o=4.5mH, C_o=1600µF.

IV. Modeling of Proposed PFC Converter Based PMBLDCM Drive

The modeling of proposed PFC converter fed PMBLDCM drive involves modeling of a PFC converter and PMBLDCM drive. The PFC converter consists of a DBR at front end and a SEPIC converter with output ripple filter. Various components of PMBLDCM drive are a speed controller, a reference current generator, a PWM current controller, VSI and a PMBLDC motor. All these components of a PMBLDCM drive are modeled by mathematical equations and the complete drive is represented by combination of these models.

A. PFC Converter

The modeling of a PFC converter involves the modeling of a voltage controller, a reference current generator and a PWM controller as given below.

1. Voltage Controller

The voltage controller is back-bone of PFC converter; therefore it affects the performance of complete drive. A proportional integral (PI) controller is used to control the DC link voltage. If at k^{th} instant of time, $V^*_{dc}(k)$ is reference DC link voltage, $V_{dc}(k)$ is sensed DC link voltage then the voltage error $V_e(k)$ is calculated as,

$$V_e(k) = V^*_{dc}(k) - V_{dc}(k) \quad (6)$$

The voltage (PI) controller gives desired control signal after processing this voltage error. The output of the controller $I_c(k)$ at k^{th} instant as derived in appendix A is given as,

$$I_c(k) = I_c(k-1) + K_{pv}\{V_e(k) - V_e(k-1)\} + K_{iv}V_e(k) \quad (7)$$

where K_{pv} and K_{iv} are the proportional and integral gains of the voltage controller.

2. Reference Current Generator

The reference inductor current of the SEPIC converter is denoted by i_{dc}* and given as,

$$I_{dc}^* = I_c(k)\,u_{vs} \quad (8)$$

where u_{vs} is the unit template of the voltage at input AC mains, calculated as,

$u_{vs} = v_d/V_{sm}$; $v_d = |v_s|$; $v_s = V_{sm} \sin \omega t$ (9)

where ω is frequency in rad/sec at input AC mains.

3. PWM Controller

The reference inductor current of the SEPIC converter (I_{dc}*) is compared with its sensed current (I_{dc}) to generate the current error $\Delta i_{dc}=(I_{dc}^* - I_{dc})$. This current error is amplified by gain k_{dc} and compared with fixed frequency (f_s) saw-tooth carrier waveform $m_d(t)$ to get the switching signals for the IGBT of the PFC converter as,

If $k_{dc}\,\Delta i_{dc} > m_d(t)$ then S = 1 (10)

If $k_{dc}\,\Delta i_{dc} <= m_d(t)$ then S = 0 (11)

where S is the switching function representing 'on' position of IGBT of PFC converter with S=1 and its 'off' position with S=0.

B. PMBLDCM Drive

The modeling of a speed controller is quite important as the performance of the drive depends on this controller. If at k^{th} instant of time, $\omega^*_r(k)$ is reference speed, $\omega_r(k)$ is rotor speed then the speed error $\omega_e(k)$ can be calculated as

$\omega_e(k) = \omega^*_r(k) - \omega_r(k)$ (12)

This speed error is processed through a speed controller to get desired control signal.

1. Speed Controller

The speed controller used in this work is a PI controller due to its simplicity. Its output at k^{th} instant is given as

$T(k) = T(k-1) + K_{p\omega}\{\omega_e(k) - \omega_e(k-1)\} + K_{i\omega}\,\omega_e(k)$ (13)

where $K_{p\omega}$ and $K_{i\omega}$ are the proportional and integral gains of the speed PI controller.

2. Reference Winding Currents

The amplitude of stator winding current is calculated as

$I^* = T(k) / (2K_b)$ (14)

where, K_b is the back emf constant of the PMBLDCM.

The reference three-phase currents of the motor windings are denoted by i_a^*, i_b^*, i_c^* for phases a, b, c respectively and given as

$i_a^* = I^*,\ i_b^* = -I^*,\ i_c^* = 0$ for $0^o \le \theta \le 60^o$ (15)

$i_a^* = I^*,\ i_b^* = 0,\ i_c^* = -I^*$ for $60^o \le \theta \le 120^o$ (16)

$i_a^* = 0,\ i_b^* = I^*,\ i_c^* = -I^*$ for $120^o \le \theta \le 180^o$ (17)

$i_a^* = -I^*,\ i_b^* = I^*,\ i_c^* = 0$ for $180^o \le \theta \le 240^o$ (18)

$i_a^* = -I^*,\ i_b^* = 0,\ i_c^* = I^*$ for $240^o \le \theta \le 300^o$ (19)

$i_a^* = 0,\ i_b^* = -I^*,\ i_c^* = I^*$ for $120^o \le \theta \le 180^o$ (20)

where θ is rotor position angle in electrical radian/sec.

These reference currents are compared with sensed phase currents to generate the current errors $\Delta i_a=(i_a^* - i_a)$, $\Delta i_b=(i_b^* - i_b)$, $\Delta i_c=(i_c^* - i_c)$ for three phases of the motor. These current errors Δi_a, Δi_b, Δi_c are amplified by gain k_1 before feeding through the PWM current controller.

3. PWM Current Controller

The PWM current controller compares these amplified current errors of each phase with carrier waveform m(t) of a fixed frequency and generates the switching sequence for the voltage source inverter based on the logic given for phase "a" as,

If $k_1\,\Delta i_a > m(t)$ then $S_a = 1$ (21)

If $k_1\,\Delta i_a <= m(t)$ then $S_a = 0$ (22)

The switching sequences S_b and S_c are generated using similar logic for other two phases of the VSI feeding PMBLDC motor.

4. Voltage Source Inverter

Fig. 3 shows an equivalent circuit of a VSI fed PMBLDCM. The output of VSI to be fed to phase 'a' of the PMBLDC motor is given as,

$v_{ao} = (V_{dc}/2)$ for $S_{a1} = 1, S_{a2} = 0$ (23)

$v_{ao} = (-V_{dc}/2)$ for $S_{a1} = 0, S_{a2} = 1$ (24)

$v_{ao} = 0$ for $I_a^* = 0$ (25)

$v_{an} = v_{ao} - v_{no}$ (26)

Using similar logic v_{bo}, v_{co}, v_{bn}, v_{cn} are generated for other two phases of the VSI feeding PMBLDC motor, where v_{ao}, v_{bo}, v_{co}, and v_{no} are voltages of three-phases and neutral with respect to virtual mid-point of the capacitor shown as 'o' in Fig. 3. The voltages v_{an}, v_{bn}, v_{cn} are voltages of three-phases with respect to neutral and V_{dc} is the DC link voltage.

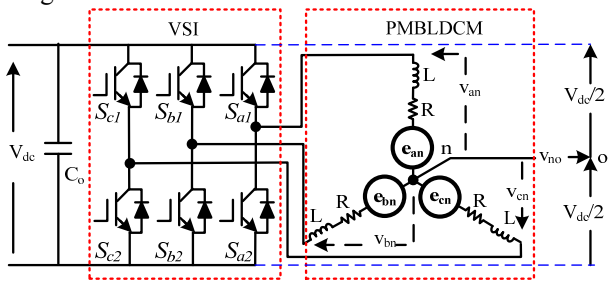


Fig. 3: Equivalent Circuit of a VSI fed PMBLDCM Drive

5. PMBLDC Motor

The PMBLDCM is modeled in the form of a set of differential equations given in Table 1.

Table 1: Modeling Equations of PMBLDC Motor

$v_{xn} = Ri_x + p\lambda_x + e_{xn}$,
$\lambda_a = Li_a - M(i_b + i_c)$;
$\lambda_b = Li_b - M(i_a + i_c)$;
$\lambda_c = Li_c - M(i_b + i_a)$
$i_a + i_b + i_c = 0$;
$v_{an} = v_{ao} - v_{no}$
$v_{no} = \{v_{ao} + v_{bo} + v_{co} - (e_{an} + e_{bn} + e_{cn})\}/3$
$\lambda_a = (L+M)\,i_a$, $\lambda_b = (L+M)\,i_b$, $\lambda_c = (L+M)\,i_c$,
$pi_x = (v_{xn} - i_x R - e_{xn})/(L+M)$
$T_e = (e_{an}\,i_a + e_{bn}\,i_b + e_{cn}\,i_c)/\omega$ and
$e_{xn} = K_b\,f_x(\theta)\,\omega$
$f_a(\theta) = 1$ for $0 < \theta < 2\pi/3$
$f_a(\theta) = \{(6/\pi)(\pi - \theta)\} - 1$ for $2\pi/3 < \theta < \pi$
$f_a(\theta) = -1$ for $\pi < \theta < 5\pi/3$
$f_a(\theta) = \{(6/\pi)(\theta - 2\pi)\} + 1$ for $5\pi/3 < \theta < 2\pi$
$T_e = K_b\{f_a(\theta)\,i_a + f_b(\theta)\,i_b + f_c(\theta)\,i_c\}$
$p\omega = (P/2)\,(T_e - T_L - B\omega)/(J)$

These equations (Table 1) represent the dynamic model of the PMBLDC motor. Various symbols used in these equations are the reference currents of the PMBLDCM for phases a, b, c are i_a^*, i_b^*, i_c^*, current error of phase "a" is Δi_a, error gain k_1 and carrier waveform for the PWM current controller m(t). Voltages of the three-phases and neutral point (n) with respect to virtual mid-point of the DC

link voltage 'o', v_{ao}, v_{bo}, v_{co}, and v_{no}, voltages of three-phases with respect to neutral point (n) v_{an}, v_{bn}, v_{cn} and the DC link voltage V_{dc} as shown in Fig. 2. R is resistance of motor/phase, L is self-inductance/phase, M is mutual inductance of motor winding/phase and x represents any of the phases a, b or c, p is a differential operator (d/dt), i_a, i_b, i_c are line currents, e_{an}, e_{bn}, e_{cn} are phase to neutral back emfs, θ is rotor position and ω=pθ is speed of PMBLDCM in rad/sec, P is number of poles, T_L is load torque in Nm, J is moment of inertia in kg-m^2 and B is friction coefficient in Nms/Rad.

V. Performance Evaluation

The proposed PMBLDCM drive is modeled in Matlab-Simulink environment and its performance is evaluated for a compressor load of an Air-Con. A constant torque load equal to rated torque mimics the compressor load of Air-Con, while running at variable speed as per requirement of air-conditioning system. The PMBLDCM of 1.2 kW, 164 V, 5 A rating, with 1200 rpm rated speed and 9.61 Nm rated torque is used to drive such load. The detailed data of the PMBLDC motor [6] are given in Appendix B. The performance of the drive is simulated for constant rated torque (9.61 Nm) at rated speed. The DC link voltage is kept constant at 400 V with an input AC rms voltage of 220 V. The components of SEPIC converter are selected on the basis of PQ constraints at AC mains and allowable ripple in DC-link voltage as discussed in Section III. The controller gains are tuned to get the desired PQ parameters and the values of controller gains are given in Appendix. The performance evaluation is made on the basis of various PQ parameters i.e. total harmonic distortion of current (THD_i) at input AC mains, displacement power factor (DPF), power factor (PF), crest factor (CF), rms value of input AC current (I_s) and efficiency (η_{drive}) of the drive.

A. Performance during Starting

Fig 4 shows that the starting of the drive is smooth with rated torque (9.61 Nm) and PFC is achieved during the starting of the drive. The motor is started from 220 V_{rms} AC input at rated torque with reference speed set at rated speed i.e. 125.7 rad/s (1200 rpm). The maximum allowable torque and the stator current during transient condition are limited to double the rated value. The motor speed reaches the reference speed within 0.1 sec. and resumes the rated value of stator current and motor torque within a cycle of AC mains frequency.

B. Performance at Variable Speeds

Figs. 5a-c show the performance of the drive during speed control of Air-Cons. The speed is increased and decreased at rated torque for detailed evaluation of the drive. The motor speed is increased to rated speed i.e. 125.7 rad/s (1200 rpm) and decreased to half the rated speed i.e. 62.85 rad/s (600 rpm) from 80% of the rated speed i.e. 100.53 rad/s (960 rpm) as shown in Figs. 5a and 5b, respectively. The motor reaches the reference speed within couple of cycles of AC mains frequency during these changes. Moreover, the motor speed is reduced to 20% of its rated value i.e. 25.13 rad/s (240 rpm) from 62.85 rad/s (600 rpm) within 0.01 sec. while achieving the PFC at input AC mains (as shown in Fig. 5c). These results validate fast control of speed, current and torque in an Air-Con with the proposed PMBLDCM drive.

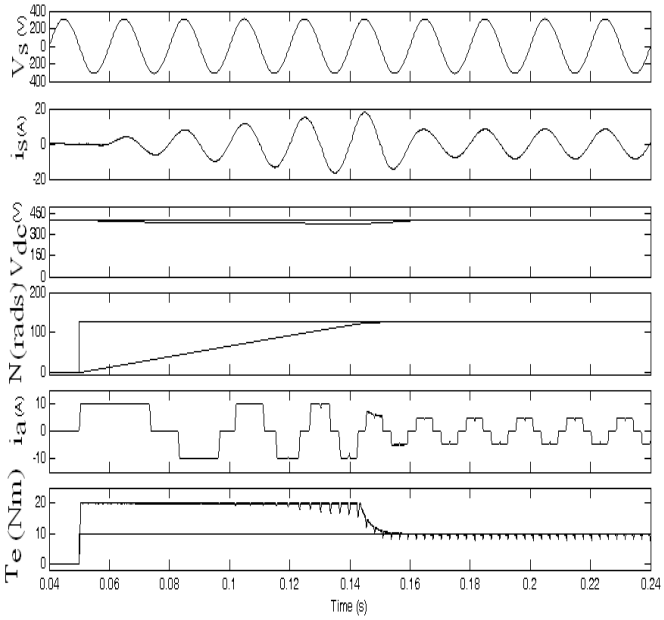
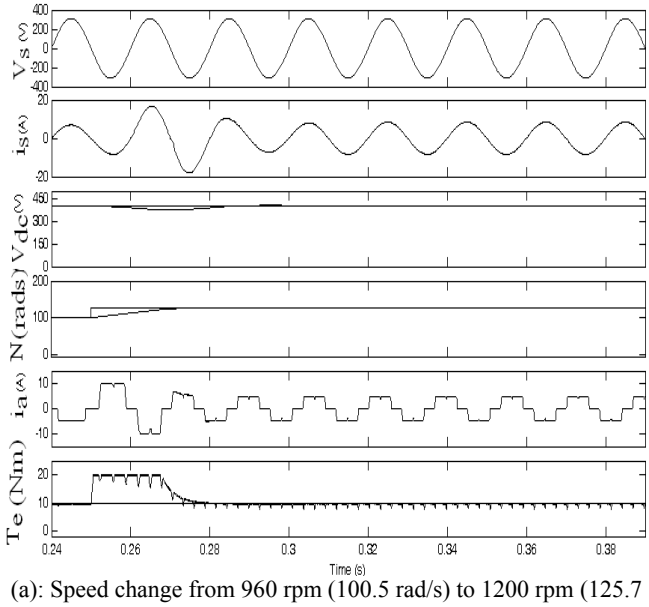
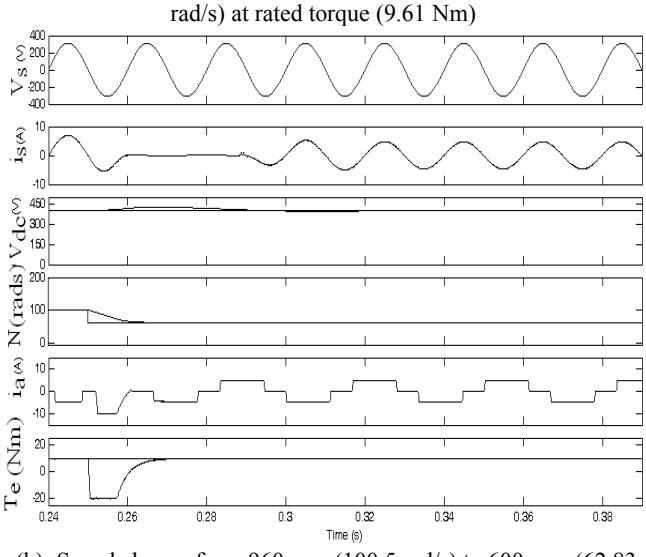


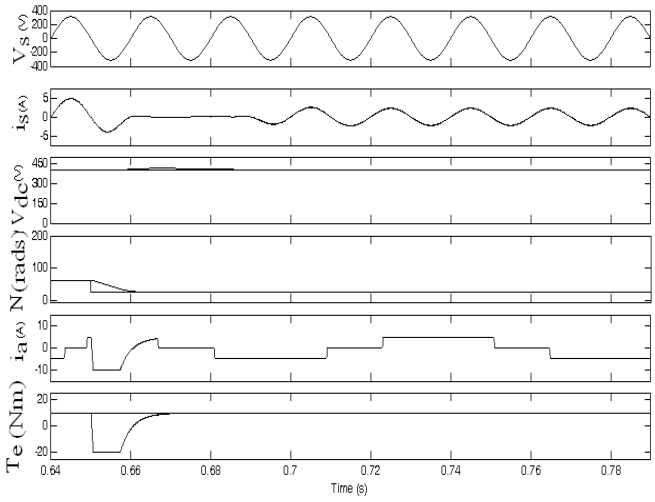
Fig. 4: Performance of a SEPIC converter fed PMBLDCM drive during Starting at rated speed i.e. 1200 rpm (125.7 rad/s) and rated torque (9.61 Nm) with 220 V_{AC} input supply



(a): Speed change from 960 rpm (100.5 rad/s) to 1200 rpm (125.7 rad/s) at rated torque (9.61 Nm)



(b): Speed change from 960 rpm (100.5 rad/s) to 600 rpm (62.83 rad/s) at rated torque (9.61 Nm)



(c) Speed change from 600 rpm (62.83 rad/s) to 240 rpm (25.13 rad/s) at rated torque (9.61 Nm)

Fig. 5: Performance of a SEPIC converter fed PMBLDCM drive during speed variation at 220 V_{AC} input supply

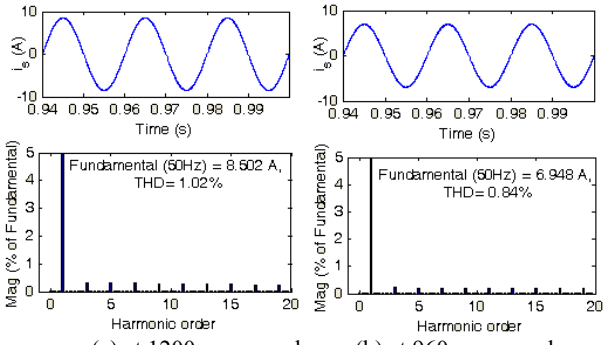
C. Performance under Steady State Condition

The current waveform at input AC mains and its harmonic spectrum during steady state at 1200 rpm (125.7 rad/s), 960 rpm (100.53 rad/s), 600 rpm (62.85 rad/s) and 240 rpm (25.13 rad/s) are shown in Figs. 6a-d. The variation of PQ parameters and drive efficiency with load (variable speed at rated torque) is shown in Table 2. The current THD at AC mains remains less than 5% with near unity power factor in the wide range of speed control of PMBLDCM drive. Moreover, an improved performance of the drive is observed in terms of reduced ripples in torque, current and speed during steady state conditions.

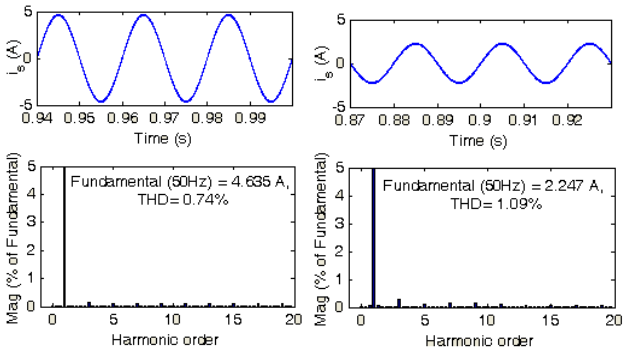
D. Performance under Input Voltage Variation

Table 3 shows the PQ parameters for variable input AC voltages (170 V-270 V) at constant DC link voltage (400 V) to the drive running at rated speed i.e. 125.7 rad/s (1200 rpm) and rated torque (9.61 Nm). These results show reduced THD of AC mains current (less than 5%) and near unity PF in wide range of input AC voltage. The efficiency of the drive remains more than 91% in the complete voltage range.

The transient and steady state performances, current waveforms and its harmonic spectra and PQ parameter variation with speed and input voltage are shown in Figs. 4-6 and Tables 2-3 to provide an exhaustive evaluation of the proposed drive system. The current THD at input AC mains in steady state conditions always remains within the standards of IEC 61000-3-2 [8] and the power factor remains near unity.



(a) at 1200 rpm speed (b) at 960 rpm speed



(c) at 600 rpm speed (d) at 240 rpm speed

Fig.6 Supply current and harmonic spectra (at 220 V_{AC}) of a SEPIC converter fed PMBLDCM drive during steady-state condition at rated torque (9.61 Nm).

Table 2: PQ parameters at variable speed and rated torque (9.61 Nm) at 220 V_{AC} input at 400 V DC link voltage

Load (%)	THD_i (%)	DPF	PF	CF	I_s (A)	η_{drive} (%)
10	1.8	0.9999	0.9999	1.41	1.02	53.5
20	1.09	1.0000	0.9999	1.41	1.59	69.1
30	0.90	1.0000	1.0000	1.41	2.15	76.5
40	0.70	1.0000	1.0000	1.41	2.72	80.7
50	0.74	1.0000	1.0000	1.41	3.28	83.8
60	0.74	1.0000	1.0000	1.41	3.83	86.1
70	0.77	1.0000	1.0000	1.41	4.37	88.0
80	0.84	1.0000	1.0000	1.41	4.91	89.4
90	0.93	1.0000	1.0000	1.41	5.47	90.4
100	1.02	1.0000	0.9999	1.41	6.02	91.3

Table 3: PQ parameters at variable input AC voltage (V_{AC}) at rated speed (1200 rpm) and rated torque (9.61Nm) at 400 V DC link voltage

V_s (V)	THD_i (%)	DPF	PF	CF	I_s (A)	η_{drive} (%)
170	2.07	0.9999	0.9997	1.43	7.79	91.3
180	1.77	1.0000	0.9998	1.41	7.35	91.3
190	1.53	1.0000	0.9999	1.41	6.97	91.3
200	1.33	1.0000	0.9999	1.41	6.62	91.3
210	1.16	1.0000	0.9999	1.41	6.30	91.3
220	1.02	1.0000	0.9999	1.41	6.02	91.3
230	0.93	1.0000	1.0000	1.41	5.76	91.3
240	0.85	1.0000	1.0000	1.41	5.52	91.4
250	0.79	1.0000	1.0000	1.41	5.30	91.4
260	0.72	1.0000	1.0000	1.41	5.09	91.4
270	0.68	1.0000	1.0000	1.41	4.90	91.4

VI. CONCLUSION

A PFC based SEPIC converter for a PMBLDCM drive has been designed for a compressor load of an air-conditioner. The PFC converter has ensured reasonable high power factor close to unity in wide range of the speed as well as input AC voltage. Moreover, performance parameters show an improved power quality with less torque ripple, smooth speed control of the PMBLDCM drive. The THD of AC

mains current is observed well below 5% in most of the cases and satisfies the international standards [8]. The performance of the drive is very good in the wide range of input AC voltage with desired power quality parameters. This converter has been found suitable for the speed control at constant torque load of air-conditioning systems.

APPENDIX A

The output of the voltage PI controller $I_c(k-1)$ [4] having K_{pv} and K_{iv} as proportional and integral gains and V_e as voltage error, is calculated at $(k-1)^{th}$ instant, as

$$I_c(k-1)=K_{pv}V_e(k-1)+K_{iv}\sum_{i=1}^{k-1}V_e(i) \quad (A1)$$

The output of the PI controller $I_c(k)$ at k^{th} instant, is

$$I_c(k)=K_{pv}V_e(k)+K_{iv}\sum_{i=1}^{k}V_e(i) \quad (A2)$$

Subtracting eqn. (a1) from eqn. (a2), the relation becomes as,

$$I_c(k)- I_c(k-1) =K_{pv}\{V_e(k)- V_e(k-1)\}+K_{iv}V_e(k) \quad (A3)$$

Therefore, the output of the PI controller $I_c(k)$ at k^{th} instant is given as

$$I_c(k)= I_c(k-1) + K_{pv}\{V_e(k)- V_e(k-1)\}+K_{iv}V_e(k) \quad (A4)$$

APPENDIX B

Rated Power: 1.2 kW, Rated Voltage: 164 V, Rated Speed: 1200 rpm, Rated Current: 5.0 A, Rated torque: 9.61 Nm, No of poles: 6, Resistance R: 1.91 Ω/ph., Inductance (L+M): 9.55 mH/ph., Torque constant K_T : 0.332 Nm/A, Inertia J= 0.00776 Kg-m^2. The Circuit Parameters used for simulations: Source impedance: 0.03 pu, Switching frequency of PFC switch = 40 kHz. The gains of voltage and speed PI controllers: K_{pv}=0.485, K_{iv}=6.85, $K_{p\omega}$=0.11, $K_{i\omega}$=1.2.

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BIOGRAPHIES

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Identification of an Effective Control Scheme for Z-source Inverter

T. Meenakshi [1] K. Rajambal [2]

Abstract – This paper presents a comparative analysis of the Z-source inverter with two different control techniques namely the simple boost control and the maximum constant boost control with third harmonic injection. The Z-source inverter has the capability to buck-boost the input voltage without any intermediate boost conversion stage. It utilizes the shoot-through states effectively to boost the input voltage. A model of the Z-source inverter is built in MATLAB/SIMULINK and its performance is analyzed with the two control schemes. The effective scheme is identified based on the current and voltage waveforms, voltage gain and voltage stress. The experimental result on a prototype inverter validates the simulation results.

Keywords – Boost factor, modulation index (M), shoot-through, voltage gain, Z-source inverter.

I. INTRODUCTION

In conventional voltage source inverters, the output voltage is always less than the input DC voltage. Also, firing the thyristors in the same leg is restricted as it short circuits the DC source [1-3]. To overcome the above said limitations, the Z-source inverter is proposed in [4]. The Z-source inverter uses a Z impedance network comprising of L and C components as the front end of the conventional inverter. The buck and boost modes of operation is achieved by adjusting the shoot through periods. Further, the shoot-through state caused by the electromagnetic interference will not destroy the circuit [5]. Therefore a more reliable single stage power converter for both buck and boost operation is obtained.

The firing scheme of the traditional PWM inverter discussed in [6]-[8] is to be modified to include the shoot through states. A simple control technique is introduced in [4] in which dc references are used to generate the shoot through state. Ref. [9] discusses the continuous and dis-continuous modes of operation of Z-source inverter using modified PWM technique. The maximum boost control technique for the Z-source inverter is explained in [10]. To reduce the current ripple and voltage stress on the inverter maximum constant boost with third harmonic injection is proposed in [11]. The digital implementation of the firing scheme is discussed in [12].

In this paper, the modeling, simulation and analysis of a Z-source inverter with two different control techniques is carried out. The firing pulses are generated using simple boost control and maximum constant boost with third harmonic injection techniques in Matlab/Simulink environment.

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The inverter is simulated with different input voltages and the effect of modulation index is studied for the firing schemes. Based on the voltage gain and voltage stress the better scheme is identified. The simulation results are validated with the prototype model.

II. Z-SOURCE INVERTER

Fig. 1 shows the circuit of the Z-source inverter. It is a buck boost inverter and has a wide range of obtainable voltage. A Z-impedance network is present at the front end of the inverter which consist of two inductors (L_1,L_2)and two capacitors (C_1, C_2) connected in X fashion. This Z-impedance network helps to boost the input voltage.

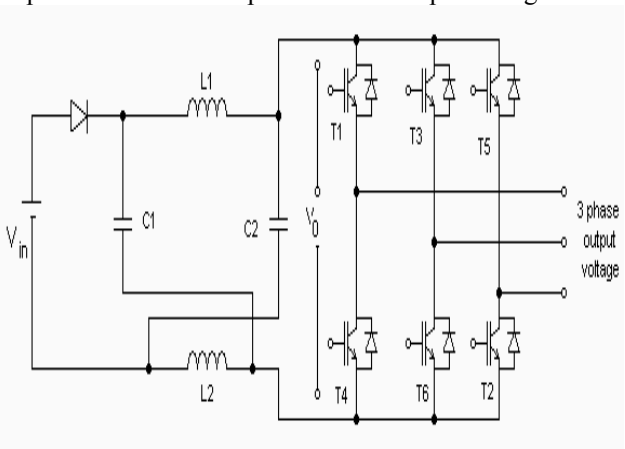


Fig. 1: Z-source inverter

The voltage boost is obtained by the introduction of shoot through states in the firing pulses. During the shoot through state, both the thyristors of the same phase leg conduct and the inverter becomes a short circuit. Fig. 2a shows the switching chart of the Z-source inverter. The shoot through period indicates the conduction of both switches in the same leg. The time period of the shoot through state is given as T_0, The time period of the non shoot through state is given as T_1. The sum of the shoot through period and non shoot period gives the total time period of the pulse (T).

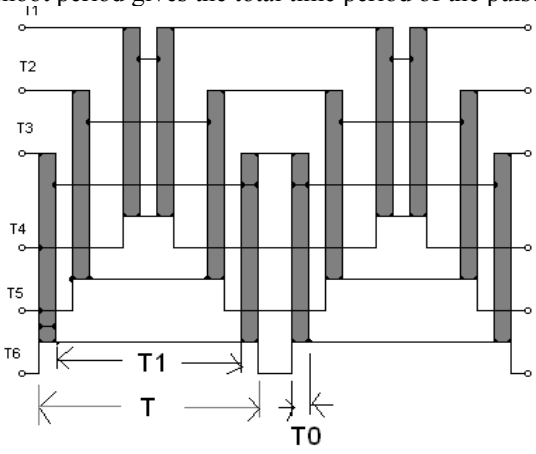


Fig. 2a: Switching chart of Z-source Inverter

The equation of the output voltage of the Z-source inverter and the boost factor is determined with the Fig. 2b. It shows the Z-source network during the shoot-through state. The inductor is energized during this state and the inductor voltage increases due to the increasing current. The capacitor is connected in parallel to the inductor and its voltage is boosted. During the non-shoot through state this boosted voltage appears across the inverter.

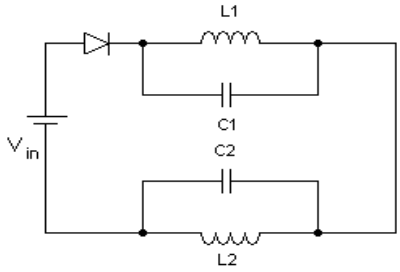


Fig. 2b: Equivalent circuit of Z-source network during the shoot through state

During the shoot through state,

$$V_L = V_c$$

and during the non shoot through state

$$V_L = V_{in} - V_c$$

where V_L is the inductor voltage, V_c is the capacitor voltage of the Z-network and V_{in} is the input DC voltage. [1]

The average voltage of inductor over one switching period is zero which is given by (1).

$$\left.\begin{aligned} V_L = \frac{T_0.V_c + T_1.(V_{in} - V_c)}{T} = 0 \\ V_c(T_0 - T_1) + T_1 V_{in} = 0 \\ V_c(T_1 - T_0) = T_1 V_{in} \end{aligned}\right\} \quad (1)$$

Based on this V_c/V_{in} is obtained as (2)

$$\frac{V_c}{V_{in}} = \frac{T_1}{T_1 - T_0} \quad (2)$$

where T_1 is the time period of non shoot through state and T_0 is the time period of shoot through state.

The capacitor voltage of the Z-network is expressed by (3)

$$V_c = \frac{T - T_0}{T - T_0 - T_0} V_{in}$$

$$V_c = \frac{1 - \frac{T_0}{T}}{1 - \frac{2T_0}{T}} V_{in} \quad (3)$$

where T denotes the total time period.

The peak DC link voltage V_0 appearing across the inverter bridge shown in Fig .1 is derived as follows and is expressed as (4).

$$\begin{aligned} V_0 &= V_c - V_L = 2V_c - V_{in} \\ &= 2\left(\frac{T_1}{T_1 - T_0}\right) V_{in} - V_{in} \\ &= \frac{T}{T_1 - T_0} V_{in} \\ V_0 &= B.V_{in} \end{aligned} \quad (4)$$

where B is the boost factor of the inverter which is given by (5)

$$\begin{aligned} B &= \frac{T}{T_1 - T_0} = \frac{1}{\frac{T_1 - T_0}{T}} = \frac{1}{\frac{T - T_0 - T_0}{T}} \\ &= \frac{1}{1 - 2\frac{T_0}{T}} \end{aligned} \quad (5)$$

T - total time period.

The output peak phase voltage obtained from the Z-source inverter is expressed as (6)

$$V_{ac} = M.V_0 / 2$$

$$V_{ac} = M.B.\frac{V_{in}}{2} \quad (6)$$

where M is the modulation index of the inverter.

3.1 Simple boost control technique

The firing pulses generated using a simple boost control scheme is shown in Fig. 3. Three sinusoidal reference signals V_a, V_b and V_c and two constant DC voltages are compared with the triangular carrier wave to generate the firing pulse with the shoot through state. The reference signals are phase displaced by 120 degrees and the amplitude of the two straight lines is equal to the peak amplitude of the reference wave.

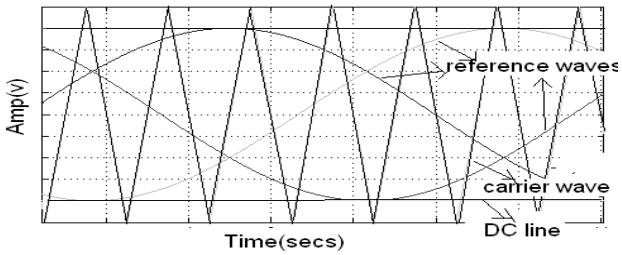


Fig. 3: Simple Boost Control scheme

When the carrier waves is greater than the upper envelope, V_p, or lower than the bottom envelope, V_n, the circuit turns into shoot-through state. Otherwise it operates as traditional carrier based PWM.

The boost factor obtained by the simple boost control technique is given by (6)

$M=T_1/T$

$$\begin{aligned} B &= \frac{1}{1 - 2T_o / T} = \frac{1}{1 - 2(T - T_1)/T} \\ &= \frac{1}{1 - 2 + 2M} = \frac{1}{2M - 1} \end{aligned} \quad (7)$$

Equation (7) gives the voltage gain obtained with the simple boost control technique.

$$G = \frac{V_{ac}}{V_{in}/2} = MB = \frac{M}{2M - 1} \quad (8)$$

The peak phase voltage of the Z-source inverter is given by (8)

$$V_{ac} = MB\frac{V_{in}}{2} \quad (9)$$

3.2 Maximum constant boost with third harmonic injection control technique

In order to reduce the cost of the Z-source network, we need to eliminate the low-frequency current ripple by using

a constant shoot-through duty ratio. The maximum constant boost control method is used to achieve maximum voltage boost while maintaining a constant boost viewed from the Z-source network. Third harmonic injection is commonly used in a three-phase inverter system to increase the modulation index range. The third harmonic injection is used here to increase the range of modulation index by which the range of voltage gain increases.

Fig. 4 shows the sketch map of maximum constant boost control with third harmonic injection. There are five modulation curves in this control method, three reference signals and two straight lines V_p and V_n. A third harmonic component with $1/6^{th}$ of the fundamental component is injected to the three phase voltage references.The upper line V_p is always equal to or higher than the maximum value of the reference signals, and the lower DC line V_n is always equal to or lower than the minimum value of the reference signals. When the carrier wave is greater than the upper line V_p or lower than the lower line V_n, shoot through periods are generated. This control method can have a modulation index from 1 to $2/\sqrt{3}$, the modulation index can be increased to more than 1. This increases the working area of the Z-source inverter. The stress on the devices is reduced in this control strategy.

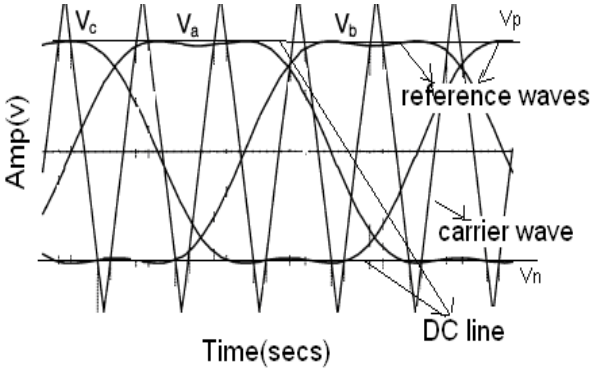


Fig. 4: maximum constant boost controls with Third harmonic Injection Technique

The shoot through duty cycle is given by (9)

$$M = \frac{2}{\sqrt{3}} T_1 / T \qquad (10)$$

$$M = \frac{2}{\sqrt{3}} (T - T_0) / T$$

$$To / T = 1 - \sqrt{3} M / 2$$

Equation (10) gives the boost factor of this technique and the voltage gain is given by (11).

$$B = \frac{1}{1 - 2To / T} = \frac{1}{1 - 2(1 - \frac{\sqrt{3}}{2} M)} \qquad (11)$$

$$= \frac{1}{\sqrt{3} M - 1}$$

The voltage gain is given by (10)

$$G = \frac{V_{ac}}{V_{in} / 2} = MB = \frac{M}{\sqrt{3} M - 1} \qquad (12)$$

III. Voltage Stress Comparison

To examine the voltage stress across the switching device V_{in} is considered to be minimum DC voltage required by the traditional voltage source inverter to obtain the same output voltage. The ratio of the voltage stress to the equivalent DC voltage for the two different control techniques is given by (12), and (13) [10].

$$\frac{V_s}{G V_{in}} = 2 - \frac{1}{G} \quad \text{for simple boost control} \qquad (13)$$

$$\frac{V_s}{G V_{dc}} = \sqrt{3} - \frac{1}{G} \quad \text{for max constant boost control} \qquad (14)$$

IV. Simulation Results

The simulation results of the Z-source inverter with the two different control techniques are discussed in this section. The Z-impedance values L and C are 200µH and 400µF respectively to obtain 415V, 50Hz AC output for an input voltage range of 200-400V. An RL load of 0.8 PF is used for study. The carrier frequency of the inverter is 10 kHz and the output filter cut-off frequency is 1 kHz.

5.1 Simple boost control Technique

The simulation results of the z-source inverter with the simple boost control technique for an input voltage of 400V are shown in Fig. 5. The Z impedance network boost the voltage to 930V (peak) for a modulation index of 0.72 which is shown in the figure 5(a). The inductor current and capacitor voltage of the Z-network is shown in the figure 5(b) and 5(c) respectively whose values are 32amps average) and 670V. The inverter output voltage is 415volts, 50Hz which is the rated value.

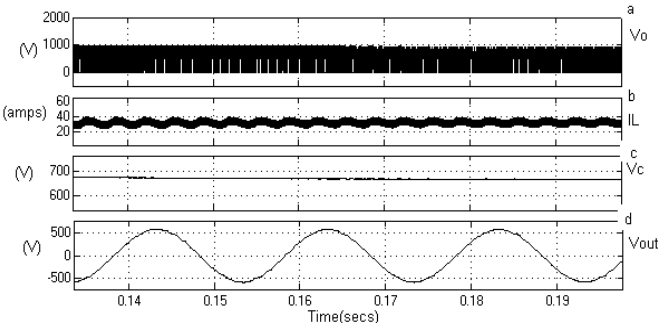


Fig. 5: Z-source inverter output waveforms with simple boost control technique

B. Maximum constant boost with third harmonic injection firing technique

To make a comparative study between the two techniques, simulation is performed using maximum constant boost control with third harmonic injection. In this method, the rated voltage of 415V (rms) is obtained at a modulation index of 0.875. The output waveforms at various stages of the Z-source inverter are shown in Fig. 6.It is observed that the input voltage is boosted to 777V (peak) by the Z-network (Fig. 6(a)). Further it is noted from Fig. 6(b) and 6(c) that the inductor current is 28 Amps (average) and capacitor voltage is 592V.

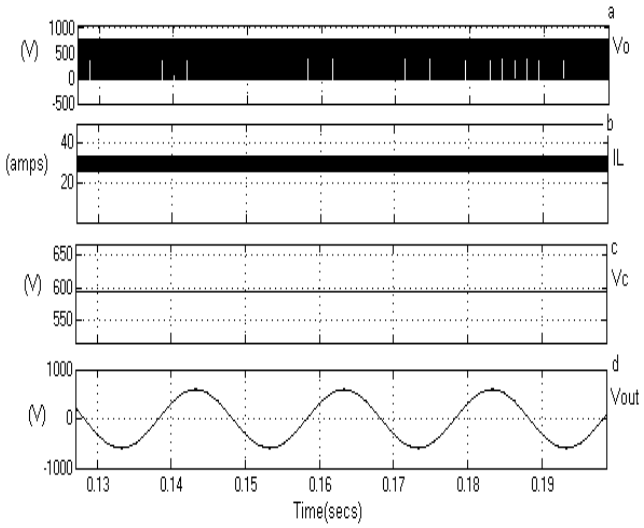


Fig. 6: Z-source inverter output waveforms with maximum constant boost control technique

To study the effect of the two control methods on the various waveforms, simulations are performed and the results are presented below.

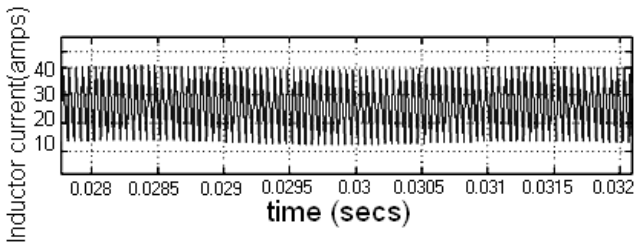


Fig. 7(a): Inductor Current profile of the Z-impedance network with simple boost control scheme

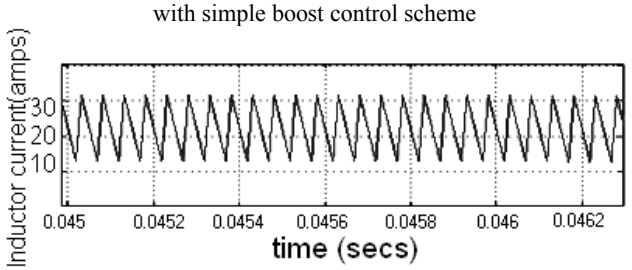


Fig. 7(b): Inductor Current profile of the Z-impedance network with maximum constant boost with third harmonic injection control scheme

Fig. 7(a) and Fig. 7(b) shows the inductor current profile obtained from the Z impedance network by the two different control schemes. It is noted that to obtain the rated voltage, the third harmonic injection scheme takes a 12.5% less inductor current than the simple boost scheme. Thus the inductor rating is reduced by the use of maximum constant boost control with third harmonic injection scheme.

The detailed view of the capacitor voltages obtained from the two control schemes for the rated voltage of 415V is shown in the Figs. 8(a) and 8(b). It is seen that for maximum constant boost control scheme with third harmonic injection the capacitor voltage is 21.5% less compared with simple boost control scheme which reduces the cost of the capacitor used.

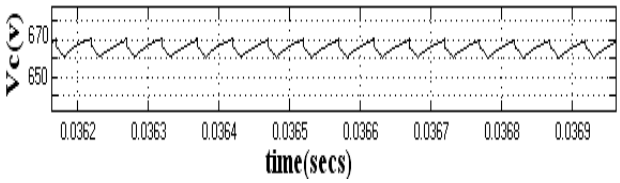


Fig. 8(a); capacitor voltage waveform of the Z-impedance network with simple boost control scheme

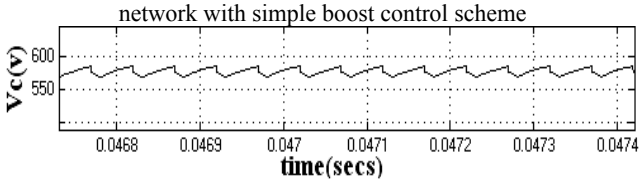


Fig. 8(b): Capacitor voltage waveform of the Z-impedance network with maximum constant boost with third harmonic injection control scheme

The output voltage waveforms without filter obtained from the Z-source inverter by the two control schemes is shown in the Figs. 9(a) and 9(b). For the same output voltage, the peak value of the output voltage with simple boost control is 800V and with that of third harmonic injection it is 632V.

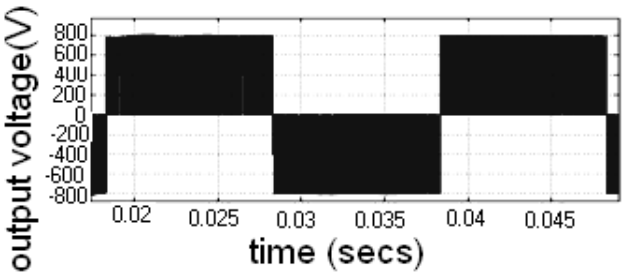


Fig. 9(a): Output voltage waveform of the Z-source inverter without filter for simple boost control scheme

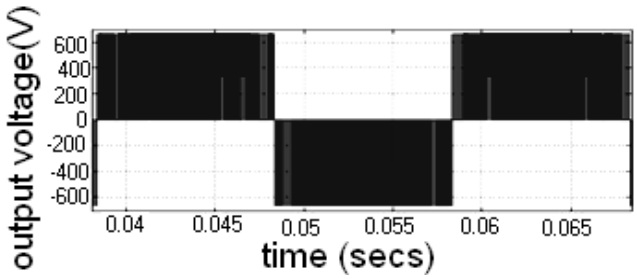


Fig. 9(b): Output voltage waveform of the Z-source inverter without filter for maximum constant boost with third harmonic injection control scheme

To make a study on the ripples present in the output current waveform of the Z-source inverter with the two different control schemes, simulations are performed to obtain the rated voltage. Fig.10(a) shows the output current waveform with simple boost control scheme and Fig.10(b) shows the output current waveform with third harmonic injection scheme. It is found that the current ripple obtained with simple boost control scheme is 9 amps whereas with third harmonic injection scheme it is 5amps. Thus the ripple present in the output current is decreased with third harmonic injection. In addition it is found that for over modulation of 1.2 with third harmonic injection scheme, The output current ripple reduces to 2amps. The reduction in the output current ripple reduces the cost of the filter used in maximum constant control with third harmonic injection scheme.

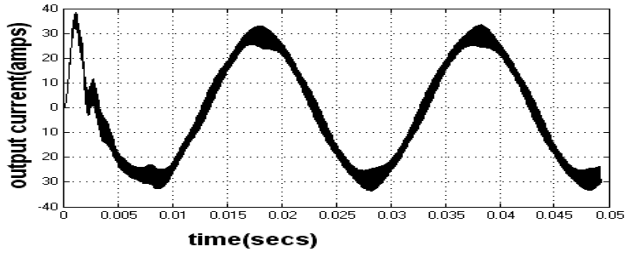


Fig. 10(a): Output current waveform of the Z-source inverter without filter for simple boost control scheme

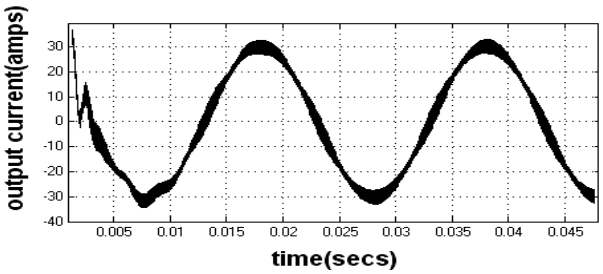


Fig. 10(b): Output current waveform of the Z-source inverter without filter for maximum constant boost with third harmonic injection control scheme

To study the harmonics present in the output voltage waveform, total harmonic distortion is obtained for the two different control schemes. The total harmonic distortion obtained with simple boost control is 3.7% and with that of third harmonic injection is 2.9%.The harmonic profile with both control scheme is shown in the Fig. 11(a)&(b). Thus there is a reduction in the THD with third harmonic injection scheme.

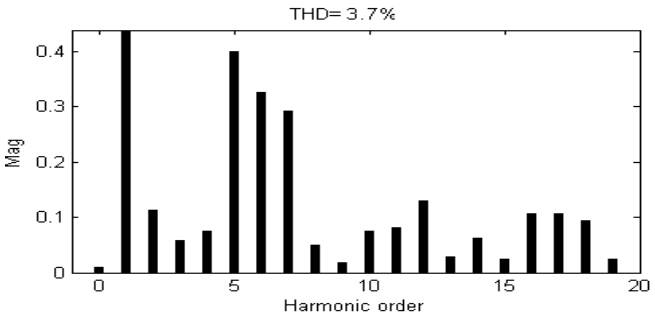
The simulation is repeated for different values of modulation index for the two control methods and the steady state output voltages are presented in Table 1.

Table 1: Comparison of Simulated Output Voltages for the Two Control Techniques, Vin=400V

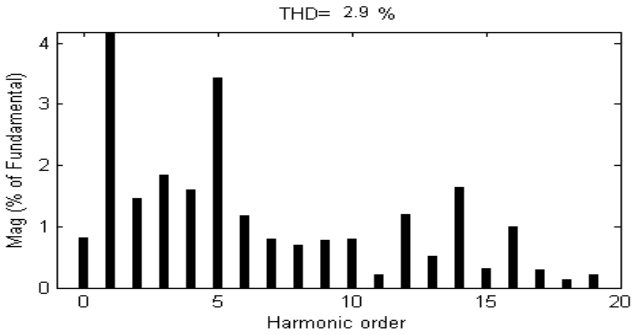
Modulation index	Simple boost control		Maximum constant boost control with third harmonic injection	
	Boost factor	V(L-L) rms (v)	Boost factor	V(L-L) rms (v)
1.15	0.762	215	1	282
1	1	255	1.366	320
0.95	1.11	264	1.54	352
0.9	1.25	275	1.79	410
0.85	1.42	303	2.12	430
0.8	1.67	326	2.59	494
0.75	2	384	3.34	597
0.72	2.27	415	4.04	700
0.7	2.5	427	4.7	782

Table 2: Comparison of Boost factor and Modulation index of the Two control Techniques

Input voltage(v)	Modulation index		Boost factor		Output voltage of Z-source inverter(v)
	SB control	MCBTHI control	SB control	MCBTHI control	
400	0.72	0.875	2.34	1.94	415
300	0.64	0.78	3.52	2.89	415
200	0.59	0.7	5.72	4.82	415



(a)



(b)

Fig: 11(a) &(b): Total harmonic distortion of the Output voltage waveform of the Z-source inverter with both control schemes

It is seen that, the output voltage increases with decreasing modulation index for both the control techniques. However the rated output is obtained at a higher modulation index in maximum constant boost control with third harmonic injection firing technique.(i.e. with a lower boost factor). As the boost factor is low, the Z impedance network requires low values of L and C. Table 2 shows the modulation index and the corresponding boost factor to obtain the rated output at different input voltages. For low values of input voltage, the shoot through period is increased to increase the boost factor. The range of boost factor is from 2.34 to 5.72 for simple boost control technique whereas it is from 1.94 to 4.82 for maximum constant boost control with third harmonic injection firing technique for an input voltage of 400V to 200V.

SB- simple boost

MCBTHI – Maximum constant boost control with third harmonic injection.

The voltage gain and stress on the devices are calculated using equation (7), (11)-(13) with different modulation index for the above mentioned control techniques at 400V input. Fig. 12 shows the variation of voltage gain with modulation index.

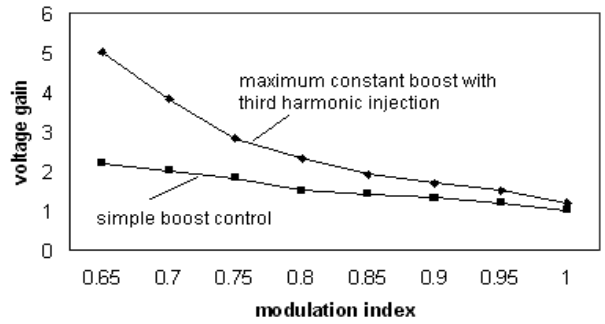


Fig. 12: Effect of modulation index on voltage gain for two control techniques

It is seen that the voltage gain is high for maximum constant boost with third harmonic injection technique. For a modulation index of 0.65, the voltage gain is 60% high compared to simple boost control technique. The difference in voltage gain decreases as the modulation index increases and they tend to be equal for modulation index greater than 1.

Fig. 13 shows the variation of voltage stress with the voltage gain.

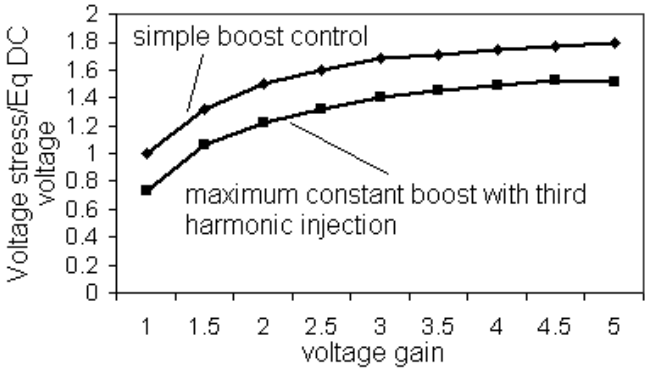


Fig. 13: Comparison of voltage stress for two control techniques

It is observed that the voltage stress developed by the maximum constant boost control with third harmonic injection is about 20% less compared to the simple boost control for the range of modulation index from 0.65 to 1.15. Therefore the maximum constant boost with third harmonic injection technique is advantageous due to the reduced voltage stress and increased voltage gain.

V. Experimental Results

A single phase Z-source inverter with maximum boost control with third harmonic injection is implemented in hardware and is shown in Fig.14. A PIC microcontroller and a PWM generator is used to generate the firing pulse with the shoot through states. The Z-parameters used in Z-source inverter for the hardware setup are L=3mH, 5A and C=470 μF, 600V. The firing pulses generated and given to the gate circuit of Z-source inverter is shown in Fig. 15. The capacitor voltage and DC link voltage for Vin=40V are 60V and 104V for a shoot through period of 0.214ms. The waveforms are shown in Fig. 16 and Fig. 17.The output voltage of Z-source inverter for the input of 40V at zero shoot through state and the 1.2ms shoot through period are 24V(peak) and 100V(peak), Vrms=72V. The output waveforms are shown in Fig. 18. The effect of shoot through period is studied and the steady state results are presented in Fig. 19.

It is seen that the output voltage increases as the shoot through period is increased and reaches a maximum of 100v(peak)volts at shoot through period of 0.214msec. It is further seen that the experimental results closely matches with the simulation results.

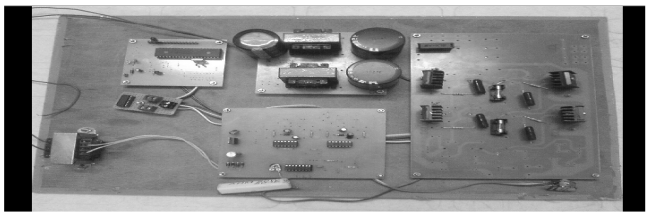


Fig. 14: Prototype Z-Source inverter

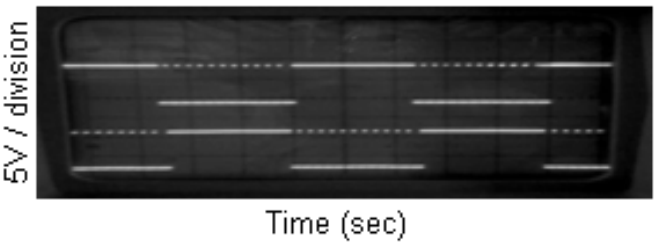


Fig. 15: Firing pulse of Z-source inverter.

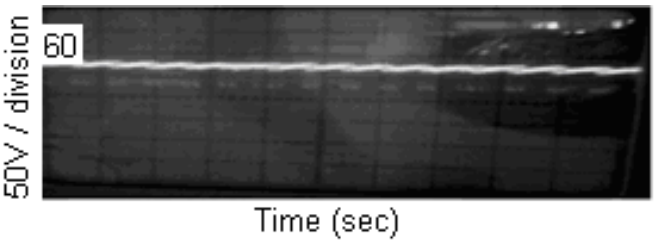


Fig. 16: Capacitor voltage of Z-source inverter.

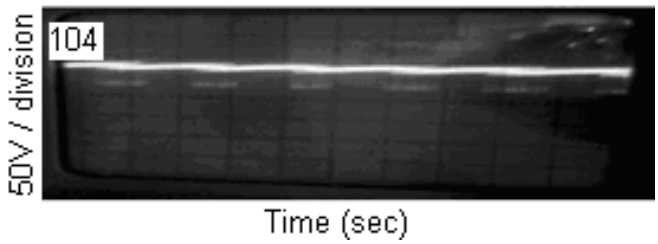


Fig. 17: DC link voltage of Z-source inverter.

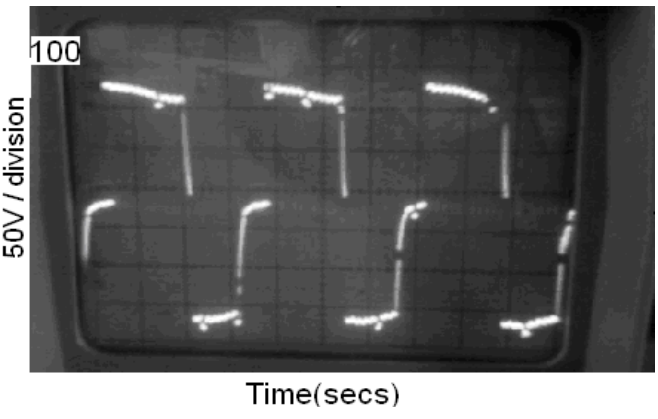


Fig. 18: Output voltage waveform of Z-source inverter.

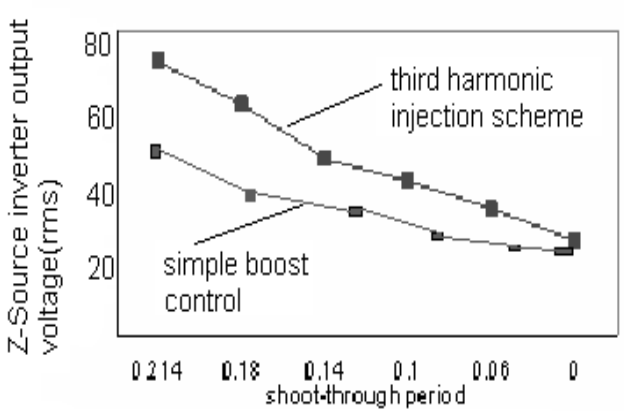


Fig. 19: Effect of shoot through period on Z-inverter output voltage for both the control schemes obtained in hardware.

VI. CONCLUSION

A simulation model of the Z-source inverter with two different control schemes namely the simple boost control and maximum constant boost with third harmonic injection control are presented. The performance of the inverter is analyzed with the two firing schemes. Based on the simulation results, it is found that the maximum constant boost with third harmonic injection technique provides the required output voltage at a low boost factor of approximately 18% less than simple boost control. The inductor current and the capacitor voltage are reduced with third harmonic injection for the same output voltage resulting in reduced L and C ratings of the Z-network. The output current ripple is also reduced by 1.8 times thus lessens the filter components used. Further, with this technique the voltage stress on the device is considerably reduced. Therefore the maximum constant boost control with third harmonic injection is identified to be the better scheme in terms of L and C requirements, voltage gain and voltage stress and implemented in hardware. The experimental results closely match with the simulation results thus validating the simulation model.

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BIOGRAPHIES

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A Fast Space-Vector Pulse with Modulation Method for Diode-Clamped Multi-level Inverter fed Induction Motor

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Abstract – This paper presents a fast space-vector pulse width modulation (SVPWM) method for five-level inverter. In this method, the space vector diagram of the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. After decomposition, all the remaining necessary procedures for the three-level SVPWM are done like conventional two-level inverter. The proposed method reduces the algorithm complexity and the execution time. It can be applied to the multi-level inverters above the five-level also. The experimental setup for three-level diode-clamped inverter is developed using TMS320LF2407 DSP controller and the experimental results are analyzed. The results have been good agreement with the published work.

Keywords – Five-level inverter, space vector pulse wide modulation, diode clamped inverter.

I. INTRODUCTION

Recent developments in power electronics and semiconductor technology have led improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have become popular and considerable interest by researcher are given on them. Three-level voltage fed PWM inverters are recently showing popularity for multi-megawatt industrial drive applications. The main reason for this popularity is that the output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion and large voltage between the series devices is easily shared [1]. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently [2], [3]. This technique results in higher magnitude of fundamental output voltage available compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states [4].

In SVPWM method the output voltage is approximated by using the nearest three output vectors that the nodes of the triangle containing the reference vector in the space vector diagram of the inverter. When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location.

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Thus the computational complexity is greatly increasing with the increasing number of the reference vectors and it is a main limitation of the application of this typical SVPWM [6],[10]. In this paper, a new method is proposed in which the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. Thus the remaining necessary procedures for the five-level SVPWM are done like conventional two-level inverter. This modification can reduce considerably the computational time and reduce the algorithm complexity. We use the redundancy of certain vectors of the space vector diagram of the inverter in order to ensure the stabilization of the input DC voltages of the inverter.

II. FIVE-LEVEL SVPWM INVERTER

Fig.1 shows diagram of a five-level diode clamping inverter. Each leg is composed of four upper and lower switches with anti-parallel diodes. Four series *dc*-link capacitors split the *dc*-bus voltage in half, and eighteen clamping diodes confine the voltages across the switches within the voltages of the capacitors. The necessary conditions for the switching states for the five-level inverter are that the *dc*-link capacitors should not be shorted, and the output current should be continuous. As indicated in Table I, each leg of the inverter can have five possible switching states, P_1, P_2, O, N_1 or N_2. When the top four witches Sx_1, Sx_2, Sx_3 and Sx_4 ($x = a, b, c$) are turned on, switching state is P_2. When the switches Sx_2, Sx_3, Sx_4 and Sx_5 are turned on switching state is P_1. When the switches Sx_3, Sx_4, Sx_5 and Sx_6 are turned on, the switching state is O. when the switches Sx_4, Sx_5, Sx_6 and Sx_7 are turned on, the switching state is N_1. When the switches Sx_5, Sx_6, Sx_7 and Sx_8 are turned on, the switching state is N_2.

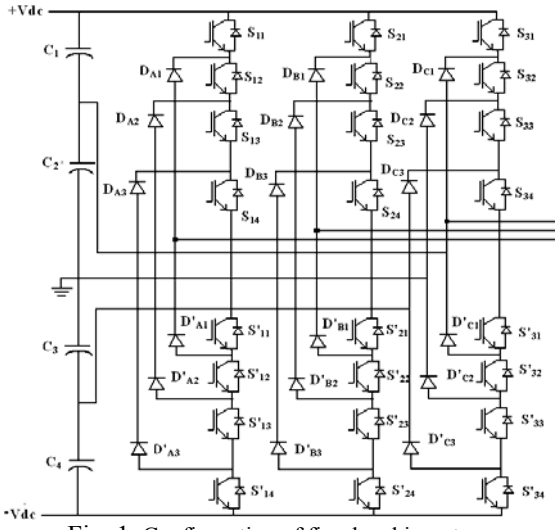

Fig. 1: Configuration of five-level inverter

Table 1: Switching states and teriminal voltages of five-level inverter

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{xo}
P_2	1	1	1	1	0	0	0	0	2E
P_1	0	1	1	1	1	0	0	0	E
O	0	0	1	1	1	1	0	0	0
N_1	0	0	0	1	1	1	1	0	-E
N_2	0	0	0	0	1	1	1	1	-2E

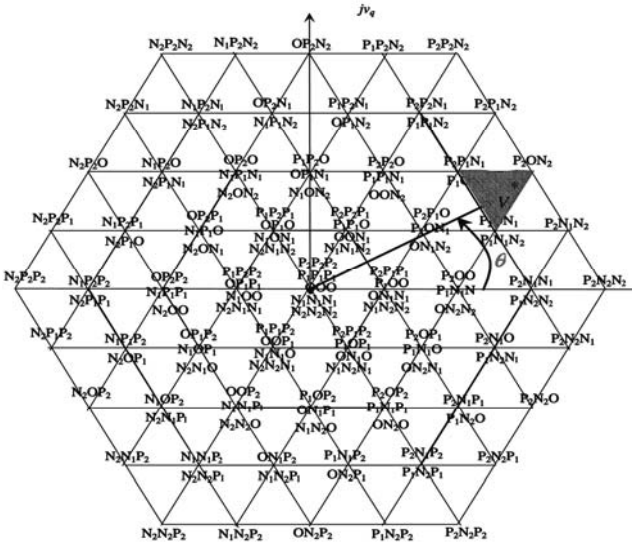

Fig. 2: Space vector diagram of five-level inverter

Fig. 2 shows the space vector diagram for five-level inverter. The output voltage space vector is identified by combination of switching states P_2, P_1, O, N_1 or N_2 of the three legs. For example, in the case of P_2ON_1, the output terminals a, b and c have the potentials $2E$, 0, and $-E$ respectively. Since five kinds of switching states exist in each leg, three-level inverter has $5^3 = 125$ switching states, as indicated in Fig. 2. The output voltage vector can take only 61 discrete positions in the diagram because some switches states are redundant and create the same space vector. In Fig. 2, it is also indicated an arbitrary reference vector V^* to be generated by the inverter.

III. FAST SPACE VECTOR PULSE WIDTH MODULATION METHOD

A. Basic Principle of Proposed SVPWM Method

The space vector diagram of multilevel inverter can be divided into different forms of sub-diagrams, in such a manner that the space vector modulation becomes more simple and easy to implement, as made in several works [5–9]. But these works do not reach a generalization of the two-level SVPWM to the case of multilevel inverters; either they divide the diagram into triangles, or into interfered geometrical forms. In this work, we present a simple and fast method that divides the space vector diagram of five-level inverter, within two steps, into several small hexagons, each hexagon being space vector diagram of two-level inverter, as shown in Fig. 3. This method is the extension of that presented in [12] for the case of three-level inverter. We have to make two simplifications: Firstly, the space vector diagram of five-level inverter is divided into six space vector diagrams of three-level inverters. Secondly, each one of these three-level inverter diagrams is divided into six space vector diagrams of two level inverters.

Thus the space vector modulation of five-level inverter becomes very simple and similar to that of conventional two-level inverter space vector modulation. To each this simplification, two steps have to be done. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the hexagons. Secondly we translate the origin of the reference voltage vector towards the centre of the selected hexagon. These steps are explained in the next section.

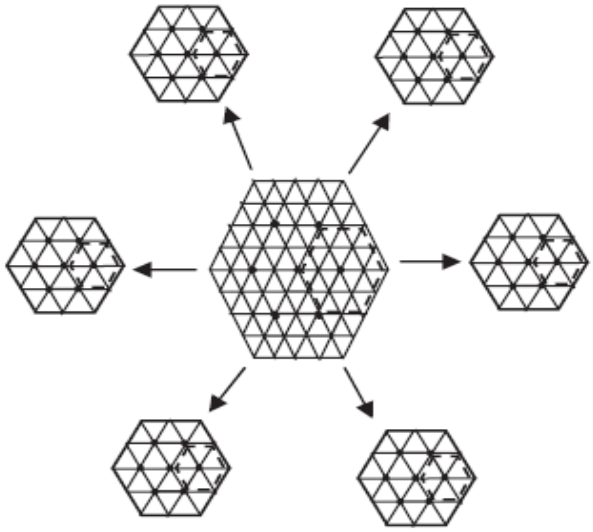

Fig. 3: Decomposition of space vector diagram of five-level inverter to six hexagons

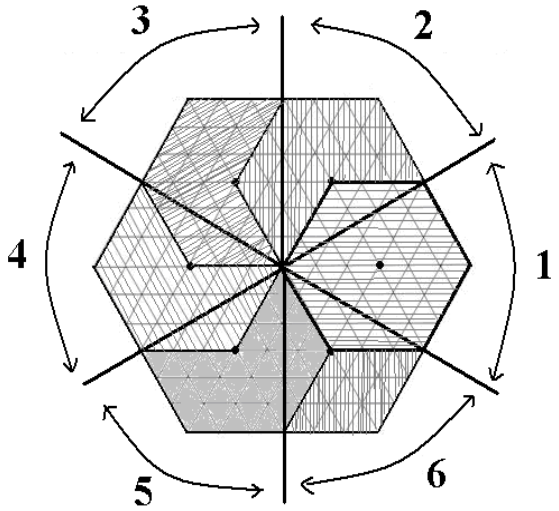

Fig. 4: Division of overlapped regions

B. First Correction of Reference Voltage Vector

Having the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that contain the five-level space vector diagram Fig. 3. There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided in equality between the two hexagons as shown in Fig. 4. Each hexagon is identified by a number s defined as given in Table 2.

Table 2: Selection of hexagons based on angle 'θ'

Hexagon 'S'	Location of reference voltage vector phase angle 'θ'
1	$-\pi/6 < \theta < \pi/6$
2	$\pi/6 < \theta < \pi/2$
3	$\pi/2 < \theta < 5\pi/6$
4	$5\pi/6 < \theta < 7\pi/6$
5	$7\pi/6 < \theta < 3\pi/2$
6	$3\pi/2 < \theta < -\pi/6$

After selection of one hexagon, we make a translation of the reference vector ***V**** towards the center of this hexagon, as indicated in Fig. 5. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table 3 gives the components *d* and *q* of the reference voltage $\mathbf{V}^{3}$* after translation, for all the six hexagons. The index (3) or (5) above the components indicate three or five-level cases respectively.

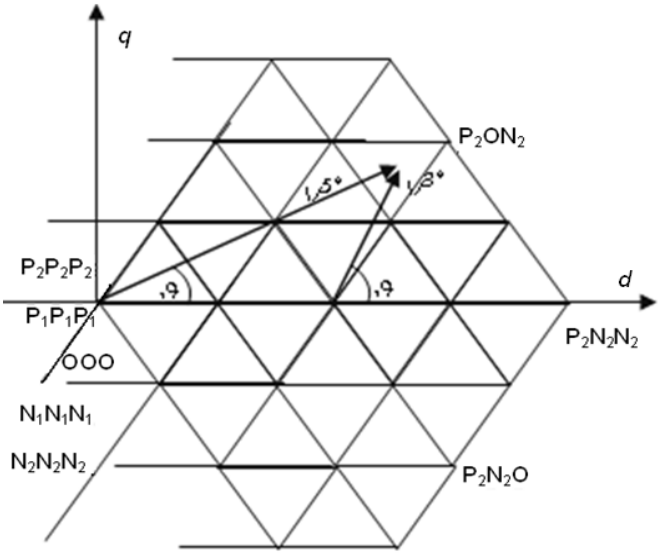

Fig. 5: First Translation of Reference Voltage Vector

Table 3: First Correction of Reference Voltage Vector

S	V_d^{3*}	V_q^{3*}
1	V_d^{5*} -1/2 cos(0)	V_q^{5*}-1/2 sin(0)
2	V_d^{5*}-1/2 cos (π/3)	V_q^{5*}-1/2 sin(π/3)
3	V_d^{5*}-1/2 cos(2π/3)	V_q^{5*}-1/2 sin(2π/3)
4	V_d^{5*}-1/2 cos(π)	V_q^{5*}-1/2 sin(π)
5	V_d^{5*}-1/2 cos(4π/3)	V_q^{5*}-1/2 sin(4π/3)
6	V_d^{5*}-1/2 cos(5π/3)	V_q^{5*}-1/2 sin(5π/3)

C. Second Correction of Reference Voltage Vector

Having the selected three-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this three-level diagram Fig. 7. Here also the overlapped regions are equally divided between the two hexagons. After selection of one hexagon, we make a translation of the reference vector V***** towards the center of this hexagon, as indicated in Fig. 7. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table IV gives the components d and q of the reference voltage V^{2}* after translation, for all the six hexagons. The index (2) or (3) above the components indicate two or three-level cases respectively.

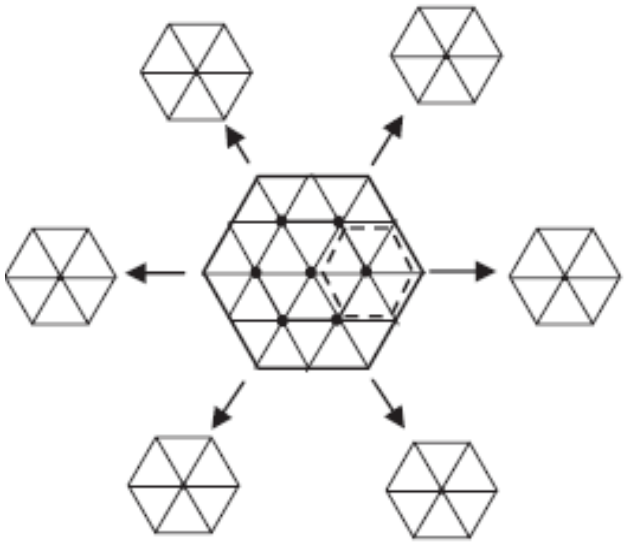

Fig. 6: Decomposition of space vector diagram of three-level inverter to six hexagons

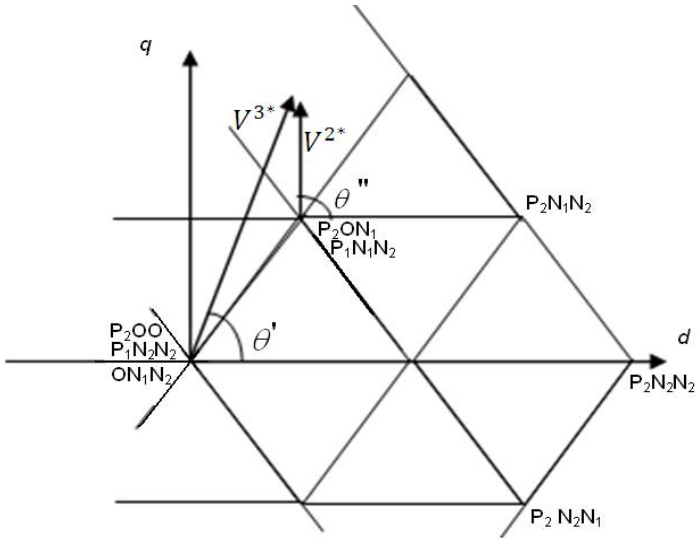

Fig. 7: Second Translation of Reference Voltage Vector

Table 4: First Correction of Reference Voltage Vector

S	V_d^{2*}	V_q^{2*}
1	V_d^{3*} -1/4 cos(0)	V_q^{3*}-1/4 sin(0)
2	V_d^{3*}-1/4 cos(π/3)	V_q^{3*}-1/4 sin(π/3)
3	V_d^{3*}-1/4 cos(2π/3)	V_q^{3*}-1/4 sin(2π/3)
4	V_d^{3*}-1/4 cos(π)	V_q^{3*}-1/4 sin(π)
5	V_d^{3*}-1/4 cos(4π/3)	V_q^{3*}-1/4 sin(4π/3)
6	V_d^{3*}-1/4 cos(5π/3)	V_q^{3*}-1/4 sin(5π/3)

D. Determination of Dwelling Times

Once the corrected reference voltage V^{2}* and the corresponding hexagon are determined, we can apply the conventional two-level space vector PWM method to calculate the dwelling times, the only difference between the two-level SVPWM and the five-level SVPWM is the factor 4 appearing at the first two equations as shown in equation 1. Since the dwelling timings of two-level inverter are divided by the value ¼. The remaining procedure is implemented like conventional two-level inverter SVPWM method and two level equivalent pulses are obtained.

$$T_1 = 4 * \left[\frac{\left| \vec{V^{2*}} \right| \cdot T_s \cdot \sin\left(\frac{\pi}{3} - \alpha \right)}{\sin\left(\frac{\pi}{3} \right)} \right]$$

$$T_2 = 4 * \left[\frac{\left| \vec{V^{2*}} \right| \cdot T_s \cdot \sin(\alpha)}{\sin\left(\frac{\pi}{3} \right)} \right] \quad (1)$$

$$T_0 = T_s - T_1 - T_2$$

E. Convertion and Sequence of the Switching States

This process is implemented by first considering each three-level decomposed space vector diagram of five-level space vector diagram based on value of 's'. Secondly, each three-level space vector diagram is further decomposed into six two-level space vector diagrams. Finally, the switching states of each two-level decomposed space vector diagrams are mapped as shown in Fig. 8 and switching states are changed in to its equivalent two-level switching states.

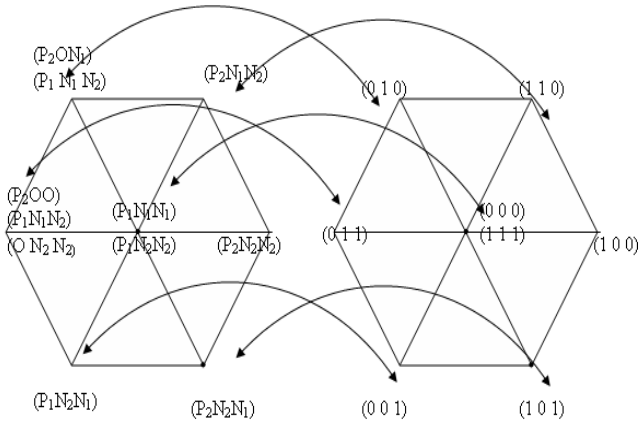

Fig. 8: Mapping of five-level switching states in to two-level switching states

The reference voltage vector V_2* is approximated using the nearest three states, which are nodes of the triangle containing the vector, identified as *X*, *Y* , and *Z*, For example, in the case of Fig. 8 , *X* is either the state P_2ON_1 or $P_1N_1N_2$, *Y* is the state P_2ON_2, while *Z* is either he state $P_2P_1N_1$ or the state P_1ON_2. The optimum sequence of these three states is selected so as to minimize the total number of switching transitions and fully optimize the harmonic profile of the output voltage. Note that from two level space vector modulation theory, it is well known that these sequences should be reversed in the next switching interval for minimum harmonic impact as given in [11-12].

Table 5: Simulation Parameters

SVPWM Parameters	Modulation index $m = 0.8$
	DC Supply voltage E = 400V
	No. of switching intervals $n = 120$
Induction motor	5.4 HP; 4 pole; 1430 rpm; $f = 50$ Hz
	$R_s = 1.405\ \Omega$; $R_r = 1.395\ \Omega$;
	$l_s = l_r = 0.005839$ H; $l_m = 0.1722$ H
SVPWM Parameters	Modulation index $m = 0.8$

IV. EXPERIMENTAL TEST SETUP

The experimental setup employed a powerful TMS320LF2407, 16-bit DSP processor working at 40 MIPS as its controller and PEC16DSMO10A, an intelligent power module (IPM) of three phase three-level diode clamped inverter. It consists of 12No's, 1200V, 50A IGBT with proper heat sink and snubber circuit. Three number of Hall Effect sensors are provided for current measurement and protection. The inverter is connected to a load of 3Ø, 0.5HP, 415V, 50 Hz, 4-pole, 1.05A, 1380 rpm induction motor and the results are obtained. The experimental setup has done only for three-level inverter as shown in Fig. 9.

Fig. 9: Experimental setup of three-level inverter

V. RESULTS AND DISCUSSIONS

In order to prove the validity of the proposed fast space vector pulse width modulation (SVPWM) method, a three phase three-level and five-level inverter fed induction motor is simulated with the simulation parameters shown in Table V. The simulation results of five-level inverter are shown in Fig. 10- 13. The gate pulses of phase A are shown in Fig. 10. The inverter output line to line voltage (V_{ab}) and its harmonic spectrum is shown in Fig. 11. The total harmonic distortion (THD) is only 0.64% and it proves the effectiveness of the proposed SVPWM method. Fig. 12 shows the load current and its harmonic spectrum. The THD of load current is decreased with increasing the level of inverter. The speed, torque and stator currents of induction motor are shown in Fig. 13. The speed and torque pulsations are reduced as comparing with two level inverter. The simulation results of three-level inverter are shown in Fig. 14 and Fig. 15. The output line to line voltage (V_{ab}) and its harmonic spectrum is shown in Fig. 14. The stator current and its harmonic spectrum of induction motor are shown in Fig. 15. In addition o the simulation results of five-level inverter, an experimental set up has developed and results are obtained for three-level inverter, when a 3Ø, 0.5HP, 415V, 50 Hz, 4-pole, 1.05A, 1380 rpm induction motor is connected as load. The output line to line voltage V_{ab} and V_{cb} are shown in Fig. 15. The induction motor load currents I_{ab} and I_{bc} are shown in Fig. 16.

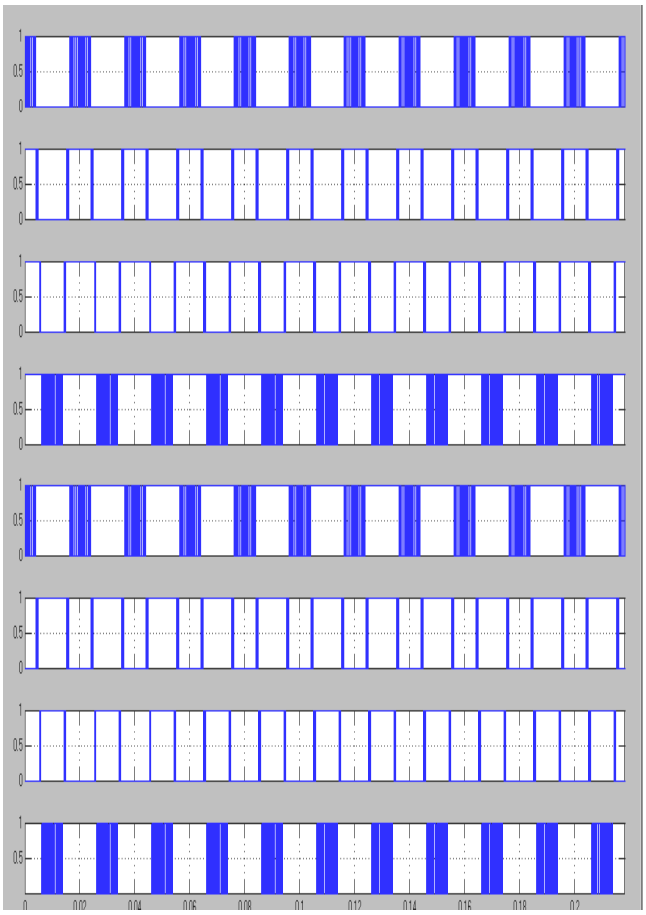

Fig. 10: Gate pulses for phase-A of five-level inverter

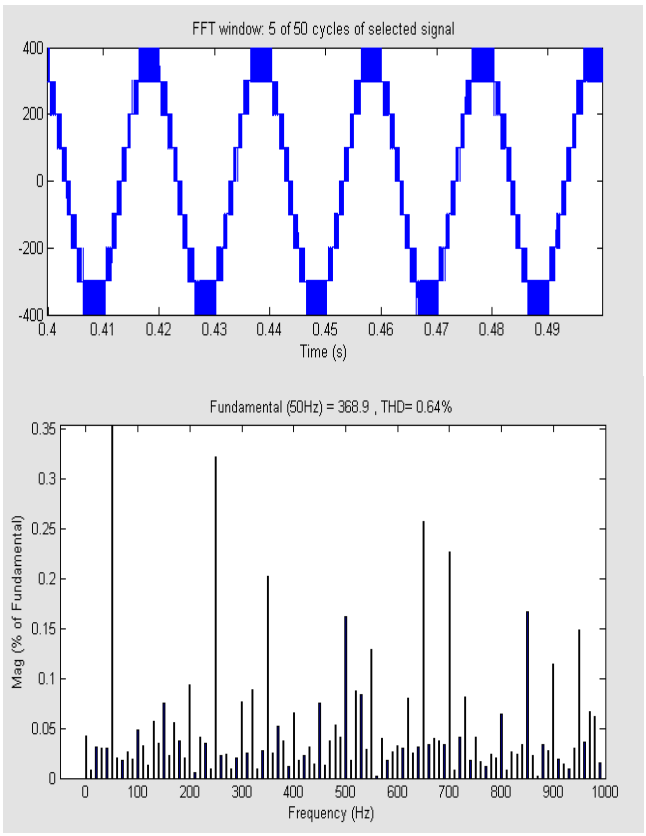

Fig. 11: The line to line voltage (V_{ab}) and its harmonic spectrum of five-level inverter

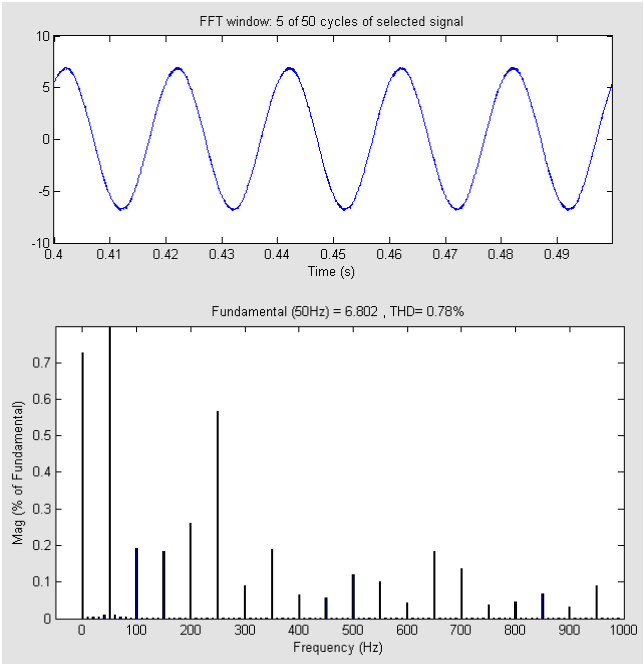

Fig. 12: The stator current I_{as} and its harmonic spectrum of five-level inverter fed induction motor

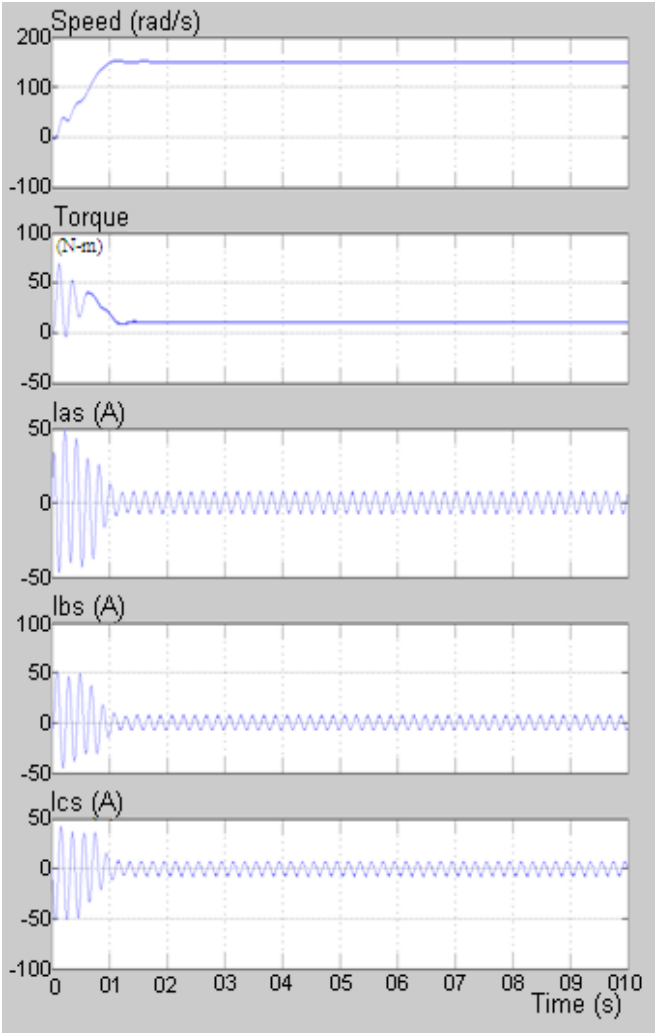

Fig. 13: Speed (N), Torque (T) and line currents Ias, Ibs, Ics of five-level inverter fed induction motor (from top to bottom)

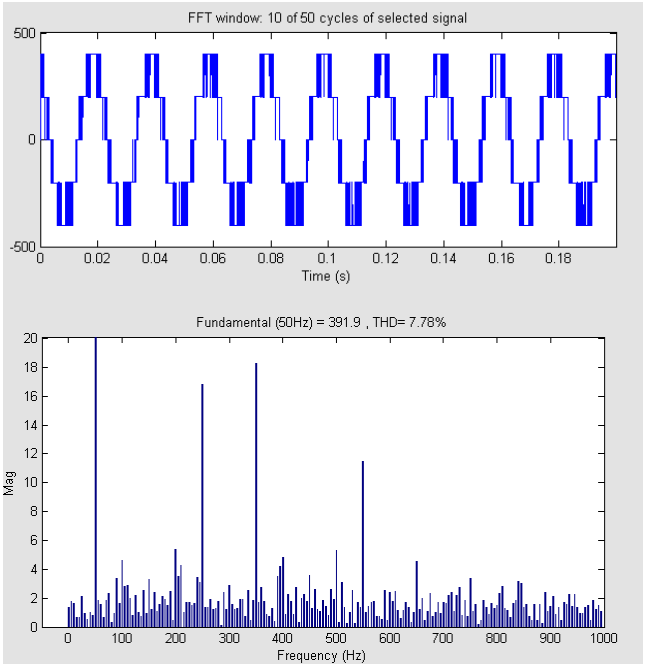

Fig. 14: The line to line voltage (V_{ab}) and its harmonic spectrum of three-level inverter

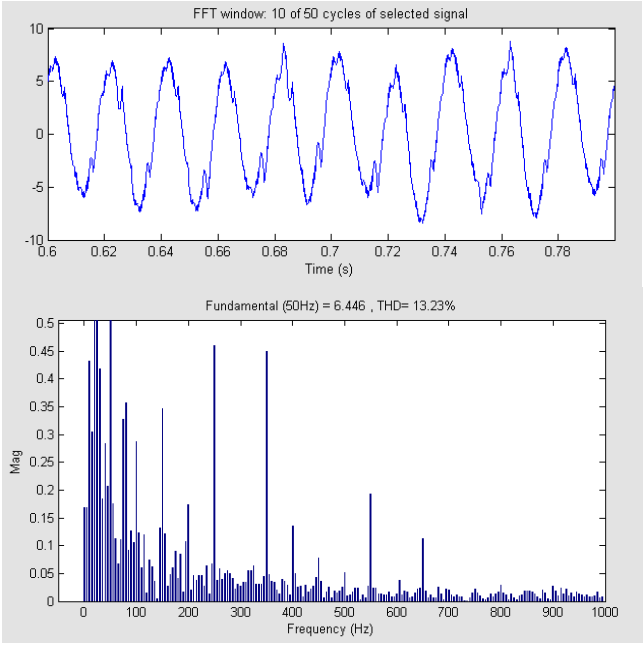

Fig. 15: The stator current I_{as} and its harmonic spectrum of three-level inverter fed induction motor

VI. CONCLUSION

In this paper, a fast space vector pulse width modulation method has been proposed and described for a five-level inverter. In this method, the space vector diagram of the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. After decomposition, all the remaining necessary procedures for the three-level SVPWM are done like conventional two-level inverter. The dwelling times of voltage vectors are calculated at the same manner as two- level inverter.

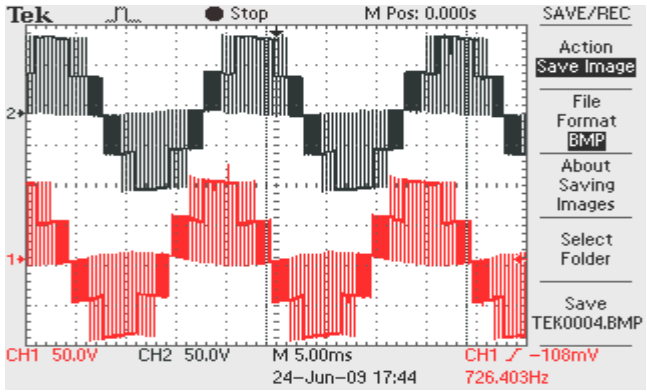

Fig. 15: The output line to line voltages V_{ab} and V_{cb} of three-level inverter

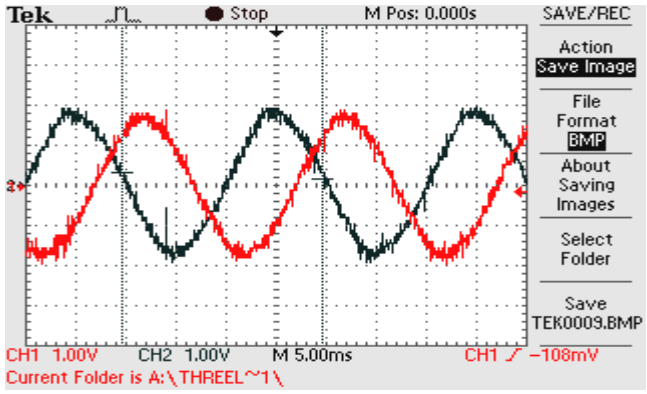

Fig. 16: The load currents I_{ab} and I_{bc} of three-level inverter fed induction motor

Thus the proposed method reduces the algorithm complexity and the execution time. It can be applied to the multi-level inverters above the five-level also. The obtained total harmonic distortion (THD) with the proposed method is only 0.64%, which is very less as compared with the other conventional methods of SVPWM techniques. The waveforms of the simulation and experimental results of three-level diode clamped inverter prove the validity of the proposed method. The results have been good agreement with the published work.

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BIOGRAPHIES

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Artificial Neural Network based Speed Control of Bidirectional Chopper fed Induction Motor Drive using DFRT Theory

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Abstract - In this paper, a new simulink model for a single phase induction motor is proposed using double field revolving theory. To maintain a constant fluid flow with a variation in the pressure head, drives like Fan load and Pump load are operated with closed loop speed control. For non linear loads, closed loop speed control is achieved using a neural network controller. A comparative study has been made between the conventional and neural network controllers. It is observed that the neural network controlled drive system has better dynamic performance, reduced overshoot and faster transient response than the PI controlled system.

Keywords - Pulse width modulation, double field Rrevolving theory, induction motor modeling, total harmonic Distortion, neural network controller.

Abbreviations

PWM	*Pulse Width Modulation*
AC	*Alternating current*
SCR	*Silicon Controlled Rectifier*
HP	*Horse Power*
DFRT	*Double Field Revolving Theory*
NN	*Neural Network*

Nomenclature

s	*Slip*
R_1	*Stator resistance in ohms*
R_2	*Rotor resistance referred to stator in ohms*
R_0	*Equivalent resistance corresponding to the iron losses in ohms*
L_1	*Leakage inductance of Stator in henry*
L_2	*Leakage inductance of Rotor referred to stator in henry*
L_0	*Magnetizing inductance of the stator in henry*
X_1	*Leakage reactance of Stator in ohms*
X_2	*Leakage reactance of Rotor referred to stator in ohms*
X_0	*Magnetizing reactance of the stator in ohms*
V_i	*Input voltage in volts*
V_0	*Output voltage in volts*
V_1	*Voltage across the variable rotor resistance in volts*
V_f	*Output voltage due to forward field in volts*
V_b	*Output voltage due to backward field in volts*
V_0	*Output voltage*
I	*Current flowing through the stator in Amps*
I_1	*Iron-loss and magnetizing component of the no-load current in Amps due to forward field*
I_2	*Rotor current referred to the stator in Amps due to forward field*
I_3	*Iron-loss and magnetizing component of the no-load current in Amps due to backward field*
I_4	*Rotor current referred to the stator in Amps due to backward field*
P_{gf}	*Airgap power developed by the motor due to forward field*
P_{gb}	*Airgap power developed by the motor due to backward field*
T	*Torque developed by the motor in Nm*
T_L	*Load Torque in Nm*
n_s	*Synchronous speed in rps*
J	*Moment of inertia in Kgm^2*
B	*Viscous friction in Nms*
P	*Number of Poles*
ω	*Angular speed in rad/sec*
θ	*Angular displacement in radians*
Y	*Output vector of the hidden layer*
O	*Output vector of the output layer*
V_{ji}	*weight matrix*
W_{kj}	*weight matrix*
B_1	*Bias vector*
B_2	*Bias vector*
X	*Input*
$a(.)$	*Activation function*
Z_j	*Activation of node j*
μ_j	*Threshold of the node j*

I. INTRODUCTION

The single-phase induction motor plays an important role in the life of industries. The advantages of this motor over other types of motor are, its simplicity, reduced cost, low maintenance and robustness. Although induction machines are the cheapest and most reliable, their controller is complex and most expensive. Due to the growing demand in improving the performance of motor drives, there is an increasing need to improve the quality and reliability of the drive circuit. The AC voltage regulator is used as one of the power electronic systems to control an output AC voltage for power ranges from a few watts up to fractions of megawatts. Phase-angle control of line-commutated voltage controllers and integral-cycle control of thyristors have been traditionally used in these types of regulators. Some techniques offer advantages such as simplicity and the ability of controlling a large amount of power economically. However, they suffer from inherent disadvantages, such as retardation of the firing angle, causing a lagging power factor at the input side, in particular, at large firing angles, and high low-order harmonic contents in both load and supply voltages/currents. AC-to-AC converter schemes using pulse width modulation (PWM) are proved to achieve substantial advantages over conventional line-commutated AC controllers. (Sadeq A. Hamed 1990, Lautaro Salazar 1993, N.A.Ahmed 1999 and M. Lucanu 2003).

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An optimal control strategy can be applied for selecting firing and commutation angles in pulse-width-modulated AC/AC chopper to eliminate selected harmonics in single-phase converters (D.A.Deib 1993, K.E.Addoweesh 1990, Yu Hongxiang 2004 and A.N.Arvindan 2006). M.J.Meco-Gutierrez (2007) has described an alternative technique, which involves the same number of commutations per unit time and therefore causes the same amount of heating in the transistors, while generating an output signal with an appreciable increase in the fundamental term and a significant reduction in lower order harmonics, which are most difficult to filter.

The double field revolving theory is effectively used to obtain the model of single induction motor. When the two fields are known the torque produced by each field can be obtained. The difference between these two is the net torque acting on the rotor. As most of the drives require constant speed operation, the firing angle is changed to maintain constant speed. The speed control in closed loop system is implemented using neural network controllers.
For controlling the speed of a single-phase induction motor, a chopper circuit is employed in the stator side (A.M. Makky 1995). The chopping switch is placed across a diode rectifier bridge, which terminates the stator winding from the opposite side to the supply. By changing the chopping frequency the rotor speed changes. The ratio of the voltage to frequency can be kept constant by using phase control in addition to the frequency control. However, remarkable speed ripples accompany low chopping frequencies. Microcontroller is used to control the speed of symmetrical pulse width modulated AC chopper fed single phase induction motor with reduced speed ripple (N.A.Ahmed 2000, S.H.Hamad 2004 and S.M.Bashi 2005). The microcontroller senses the speed's feedback signal and consequently provides the pulse width variation signal that sets the gate voltage of the chopper, which in turn provides the required voltage for the desired speed.

As long as the parameters of PID control, proportional gain, integral time, differential time and sampling period are optimized and tuned, conventional PID control obtains better performance and higher control precision. However, the robustness of PID is reduced when the parameters of the model are varied. The neural network PID control, which is a method for adaptively adjusting the PID gains using backpropagation algorithm can be adopted. The neural network PID control has the capability of self-study and self-adaptation (Y.S.Kung 1995 and Jiangjiang Wang 2007).

A control technique based on a neural network is proposed here for the constant speed control of the single phase induction motor drive. In the industry, the PI controller is widely used. These controllers exhibit excellent ability if a simple control is to be implemented. However, they have low reliability because these control results are sensitive to change in system parameters and do not react rapidly to parameter changes. Also, these controllers show a higher maximum overshoot and longer settling time. To solve these problems, a neural network that adjusts itself to control circumstances, is used.

Various kinds of neural network architecture is studied (B.K. Bose 2001). Most of the current ANN applications are restricted to feed forward back propagation type network. Off-line trained artificial neural networks are applied for creating the system inverse models that are used at designing control algorithm for non-linear dynamic system (O.Bouhali 2005 and Jaroslava Zilkova 2006). Backpropagation neural networks find application in a self-tuning adaptive control of unknown, non-linear and feedback linearizable plants. (Kulawaki G. J.1994)
The above literatures does not deal with neural network based closed loop control of bidirectional chopper fed induction motor drive systems. In the present work, the simulation has been performed for both phase controlled and pulse width modulated chopper systems. From the simulation, it is proved that the performance of pulse width modulated AC chopper system is superior to phase controlled AC chopper system. A new simulink model of single phase induction motor using double field revolving theory is proposed. Artificial neural network based closed loop speed control is proposed for the single phase induction motor.

II. BIDIRECTIONAL CHOPPER FED INDUCTION MOTOR

A block diagrammatic representation of a neural network controlled AC chopper fed single phase induction motor is shown in Fig. 1. The circuit can operate directly from a single phase line and the voltage across each switch is limited to the line voltage. Various parameters, namely, pulse width modulated voltage, stator current, speed of the induction motor and error in speed are sensed and given to the neural network. It generates the driving pulses to the switches in order to maintain the speed of the machine at reference value. A neural network is proposed for speed regulation. During each time, the weights and biases of the neural network are updated using the back propagation algorithm to make the error between the desired outputs and actual outputs of the neural network less than the predefined value.

The neural network controller has a 6-3-1 structure. This neural network structure is the result of many repeated trials. For each load, the training data is obtained by tuning the PI controller parameters such as k_p, k_i to optimal values in order to obtain a small steady-state error.

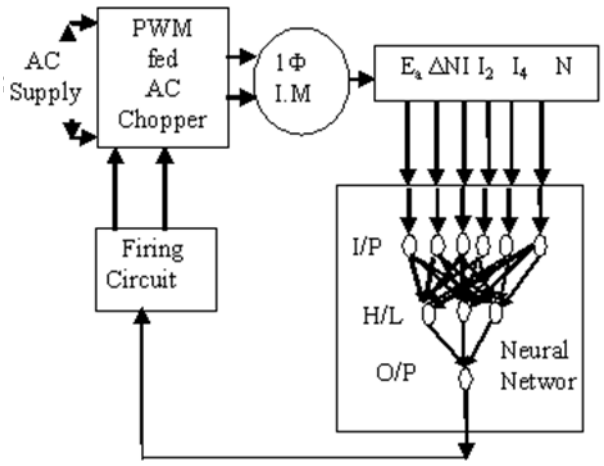


Fig. 1: Block diagram of single phase induction motor with neural network controller

The neural network controller is capable of maintaining a good steady-state and dynamic responses, and shows a significant improvement in reducing the distortion of the output voltage under non-linear loading conditions. It is suitable for the applications where the load undergoes periodic distortions.

III. Simulink Model of Single Phase Induction Motor

The equivalent circuit of the single phase induction motor is considered to derive the simulink model of it. Since the value of slip (s), is generally small, $R_2/2s$ is considerably higher than $R_2/[2*(2-s)]$. In general, the magnitude of V_f (V_0-V_b) is 90% to 95% of the applied voltage.

Current flowing through the stator is expressed as

$$I(s) = \frac{(V_i(s) - V_0(s))}{(R_1 + sL_1)} \quad (1)$$

A. Model for Forward Field

Current flowing through the stator can be expressed as

$$I(s) = I_1(s) + I_2(s) \quad (2)$$

If the rotor current referred to the stator is taken as I_2, then the iron-loss and magnetizing component of the no-load current can be expressed as

$$I_1(s) = I(s) - I_2(s) \quad (3)$$

The forward field voltage can be obtained from the expression

$$V_f(s) = V_0(s) - V_b(s)$$
$$= \{I_1(s)\}\left\{\frac{sR_0L_0}{(R_0 + sL_0)}\right\} \quad (4)$$

It can be rewritten as

$$V_f(s) = V_0(s) - V_b(s) \quad (5)$$

$$= \{I_1(s)\}\left\{R_0 - \left[\frac{R_0^2}{(R_0 + sL_0)}\right]\right\}$$

Voltage across the rotor inductance is expressed as

$$V_1(s) = \{V_f(s) - I_2(s)\}\left(\frac{R_2}{s}\right) \quad (6)$$

The rotor current referred to stator can be expressed as

$$I_2(s) = \frac{[V_f(s) - V_1(s)]}{sL_2} \quad (7)$$

Airgap power developed by the motor is given by the expression

$$P_{gf}(s) = \{[I_2(s)]^2\}\{\frac{R_2}{s}\} \quad (8)$$

A. Model for Backward Field

Current flowing through the stator can be expressed as

$$I(s) = I_3(s) + I_4(s) \quad (9)$$

If the rotor current referred to the stator is taken as I_4, then the iron-loss and magnetizing component of the no-load current can be expressed as

$$I_3(s) = I(s) - I_4(s) \quad (10)$$

The forward field voltage can be obtained from the expression

$$V_b(s) = \{I_3(s)\}\left\{\frac{sR_0L_0}{(R_0 + sL_0)}\right\} \quad (11)$$

It can be rewritten as

$$V_b(s) = \{I_3(s)\}\left\{R_0 - \left[\frac{R_0^2}{(R_0 + sL_0)}\right]\right\} \quad (12)$$

Voltage across the rotor inductance is expressed as

$$\{V_b(s) - I_4(s)\}\left(\frac{R_2}{(2-s)}\right) \quad (13)$$

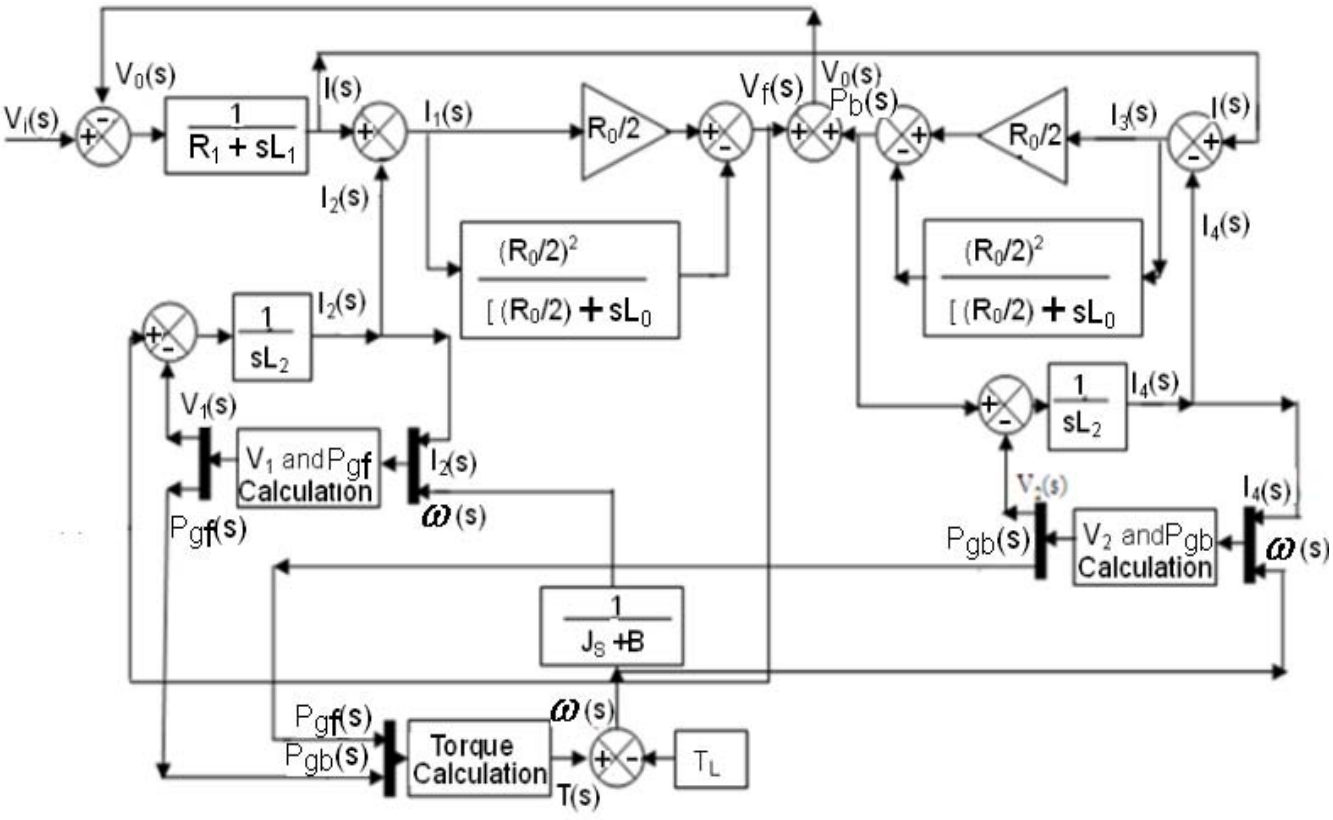


Fig. 2: Simulink model of single phase induction motor using DFRT

The rotor current referred to stator can be expressed as

$$I_4(s) = \frac{[V_b(s) - V_2(s)]}{sL_2} \quad (14)$$

Airgap power developed by the motor is given by the expression

$$P_{gb}(s) = \{[I_4(s)]^2\}\{\frac{R_2}{(2-s)}\} \quad (15)$$

Torque developed by the motor is given by the expression

$$T(s) = \frac{P_{gf}(s) - P_{gb}(s)}{2\pi n_s} \quad (16)$$

The load balance equation is given by

$$\omega(s) = \frac{(T(s) - T_L(s))}{Js + B} \quad (17)$$

From (1) – (17), the model for the single phase induction motor is obtained. The proposed model is shown in Fig. 2. A 1 HP, 230V Single phase induction motor with the following parameters is used for simulation.

R_1=3.4Ω X_1=3.45Ω R_2=1.6Ω
X_2=3.45Ω R_0=170.58Ω X_0=76.44Ω
J=0.0146kgm^2 B=0.00365Nms

IV. Neural Network Controller

Neural networks are simply a class of mathematical algorithms, since a network can be regarded as a graphic notation for a large class of algorithms. The hidden layer transfer function is log-sigmoid or tan-sigmoid and the output transfer function is usually linear. Here, the tan-sigmoid is used as the hidden layer transfer function followed by the linear transfer function for the output layer. The neural network system to estimate the duty ratio of AC chopper fed single phase Induction Motor is shown in Fig. 3.

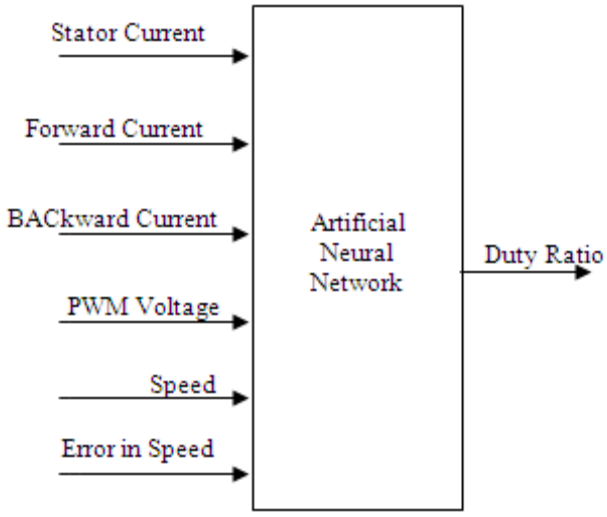


Fig. 3: Neural Network system to estimate duty ratio of PWM AC Chopper fed Single Phase Induction Motor

Output of each hidden node j is given in (18).

$$Y_j = a(Z_j) \quad (18)$$

Where a(.) is termed the activation function and the expression for Z_j is given in (19).

$$Z_j = \sum_i V_{ji} X_i + \mu_j \quad (19)$$

is termed the activation of node j and it is the weighted sum of the inputs X_i to that node and μ_j is termed the threshold of the node. The most commonly used activation function is the sigmoid function and given in (20).

$$a(Z) = 1 \Big/ \left(1 + e^{-z}\right) \quad (20)$$

The output of each output node is linear and is given in (21).

$$O_k = \sum_j W_{kj} Y_j \quad (21)$$

Where V_{ji} and W_{kj} are weights of hidden and output layers.

Equations 22 and 23 show the transfer functions, where X is the input vector, Y and O are the output vectors of the hidden layer and output layer respectively. V_{ji}, W_{kj} are the weight matrices, and B_1 and B_2 are the bias vectors.

$$Y = 1 \Big/ \left(1 + e^{-(V_{ji}.X + B_1)}\right) \quad (22)$$

$$O = (W_{kj})(Y) + B_2 \quad (23)$$

To provide the required data to train the neural network, a simulation program is written to obtain the duty ratio values for different load torques. Using this programme, 1,00,000 sets of training pattern such as pulse width modulated output voltage, stator current, speed of the machine, load torque and duty ratio values are obtained. These patterns are used for training the neural network using error back propagation algorithm. After training the neural network successfully, the program is replaced by neural network controller and the simulation has been performed. Output of the neural network controller is used to vary the duty ratio of the PWM AC chopper.

V. Closed Loop Stator Voltage Controlled Single Phase Induction Motor

The neural network based closed loop stator voltage control of a single phase induction motor system is shown in Fig. 4. The power circuit used to generate the Pulse Width Modulated AC voltage is modeled and simulated. PWM AC voltage is applied to the single phase induction motor and the speed is sensed by using a speed sensor. The actual speed of the motor is compared with the reference speed, which can be set by the industrial user according to his requirement. The error in speed is given to the PI controller with a saturator. Initially, PI controllers are used to control the voltage applied to the single phase induction motor. The values of k_P and k_I are tuned for various load conditions. For each load, the PI controller is tuned to obtain a constant speed, and parameters like pulse width modulated output voltage, stator current, speed of the machine, error in speed and duty ratio are estimated. Around 1,00,000 sets of training patterns are obtained. These patterns are used for training the neural network, using the error back propagation algorithm. The internal structure of the trained neural-network used for the simulation is shown in Fig. 5.

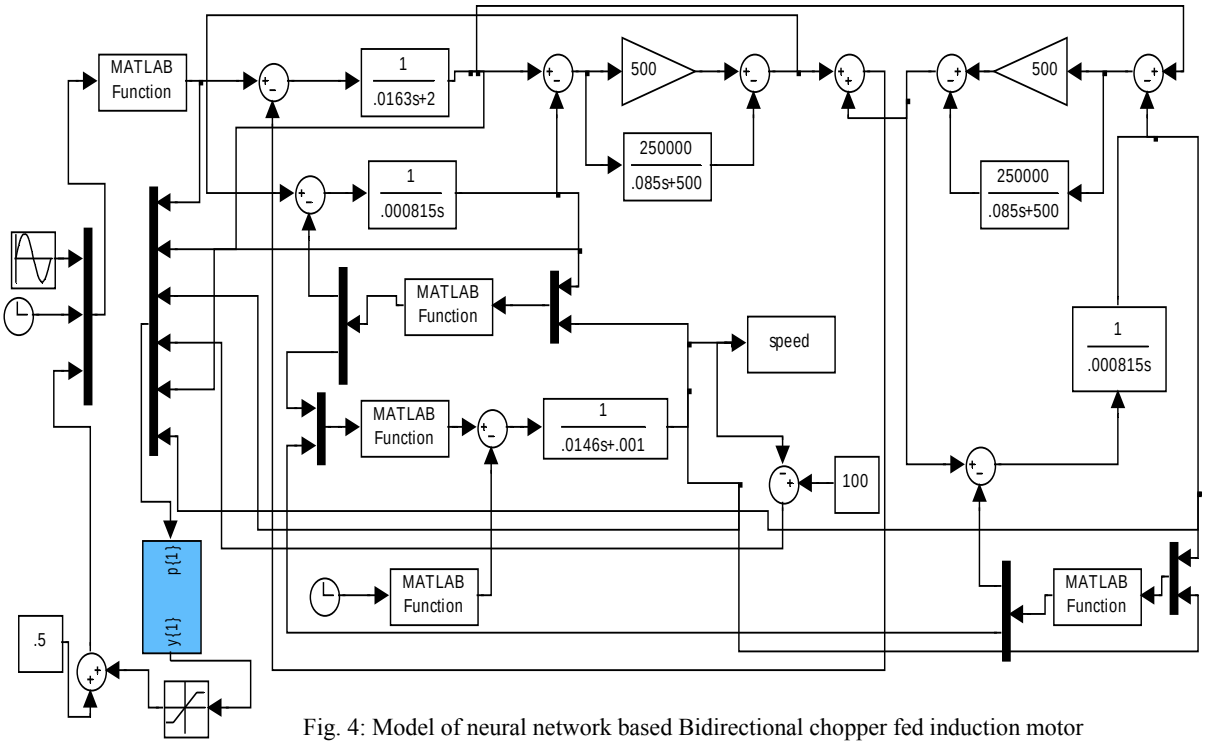
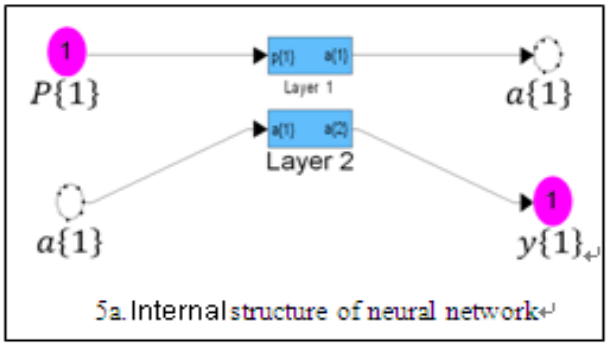
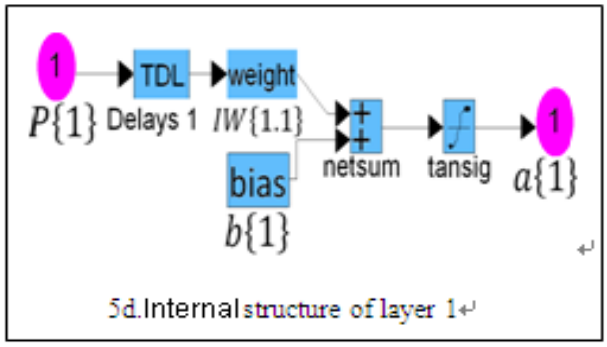


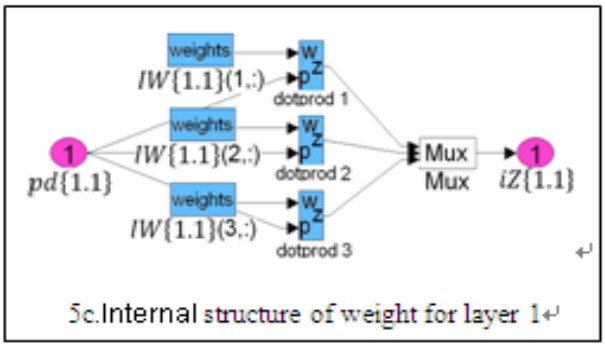
Fig. 4: Model of neural network based Bidirectional chopper fed induction motor



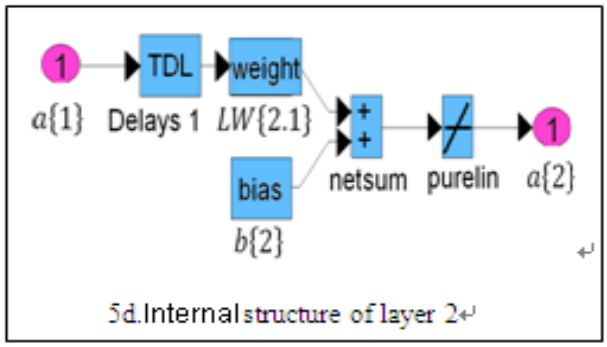
5a. Internal structure of neural network



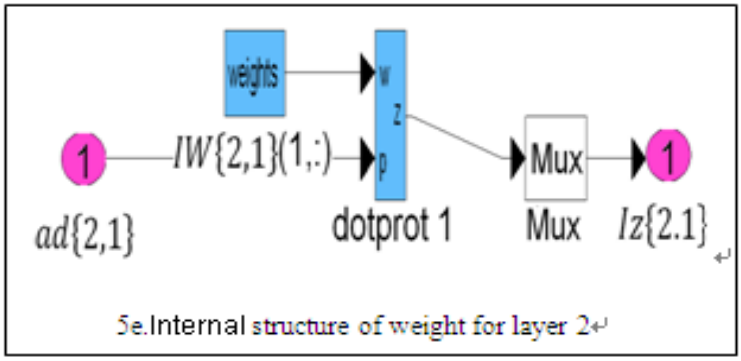
5d. Internal structure of layer 1



5c. Internal structure of weight for layer 1



5d. Internal structure of layer 2



5e. Internal structure of weight for layer 2

Fig. 5: Internal structure of the trained neural-network

After training the neural network successfully, the conventional PI controller is replaced by the neural network controller and the simulation is performed. The output of the neural network controller is used to vary the duty ratio of the PWM AC chopper. Non-linear exponential load is considered. The speed response for the open loop system from no load to maximum load torque is shown in Fig. 6. From Fig. 6, it can be seen that the speed

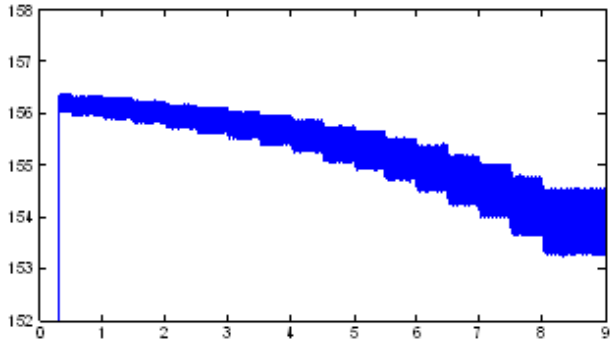


Fig. 6: Speed response with open loop system

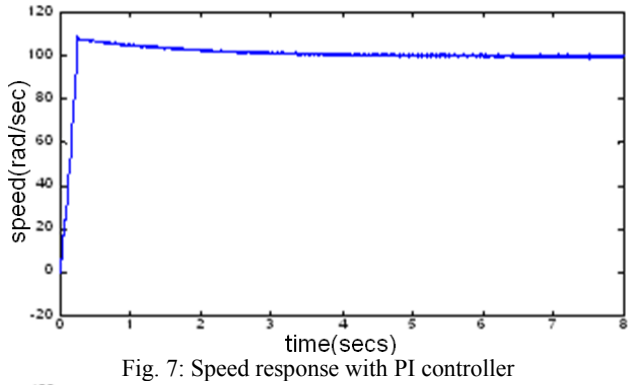


Fig. 7: Speed response with PI controller

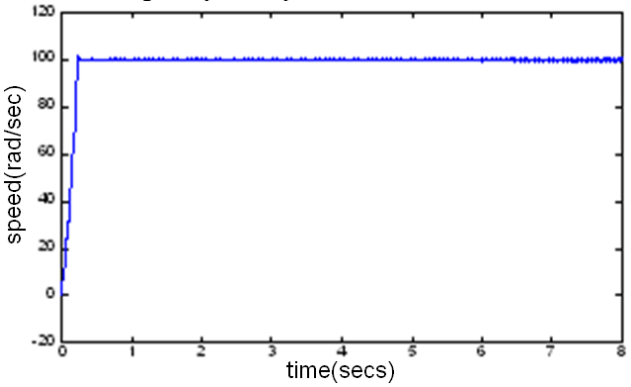


Fig. 8: Speed response with neural network

is not constant in the open loop system. The speed at no load is 156.4rad/sec. As the load is increased, the speed decreases, and finally, it reaches 153.2rad/sec for full load. The speed is maintained at reference value irrespective of the load torque with a closed loop stator voltage control. The speed is maintained constant as shown in Figs. 7 and 8 for non-linear variation of load torque. The simulation is carried out for a reference speed of 100 rad/sec. The speed is maintained at 100rad/sec using PI and NN controllers. The steady state error is reduced. Thus, the closed loop system is capable of maintaining the speed at constant value. The simulation results obtained by using the neural network and PI controllers are given in Table 1.

Table 1: Comparison of Neural Network and PI Controller based Induction Motor Drive systems

Parameters	Neural Network	PI Controller
Rise time(sec)	0.2	0.274
Settling time(sec)	0.2636	4
Peak Overshoot(%Mp)	1.9608	9.091

From the above table, it can be seen that the neural network has lesser peak overshoot, reduced rise and settling time.

VI. CONCLUSION

The Pulse Width Modulated AC Chopper and the Phase Angle Controlled AC Chopper fed Induction motor systems are simulated and their performances are compared. It is proved that the Pulse Width Modulated AC Chopper has lesser total harmonic distortion, better power factor and negligible harmonic components.

Modeling of an Induction Motor has been done using double field revolving theory and the closed loop control has been analyzed. An intelligent control system using a neural network controller has reduced peak overshoot, rise time and settling time compared to the system with a PI controller. It is observed that the speed of the machine remains constant with reduced overshoot by using the neural network-based controller.

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